I B.Sc.,(CBCS),I-Sem. Unit-I: A C CIRCUIT FUNDAMENTALS

The Sinusoidal voltage/current wave – Average and RMS value– Phasor representation - 'J' operator, A C applied to RC, RL and RLC circuits – Phasor diagrams- concept of impedance- Power factor in AC circuits – Numerical problems.

Introduction: AC voltages and currents are generated by rotating a coil of wire (rotor) inside a magnetic field (stator), as shown in Fig.(1), the resulting waveform is a sine wave as shown in Fig.(2). The height or amplitude of a sine wave is called the Peak value. It is often described by Effective or Root-Mean-Square (RMS/rms) value and Average value. The RMS value is about 70.7% of the Peak value and the Average value is 63.7% of the peak value. Most analog and digital meters measure RMS value of a sine wave.

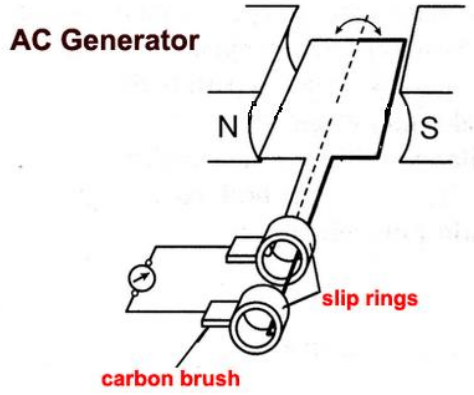
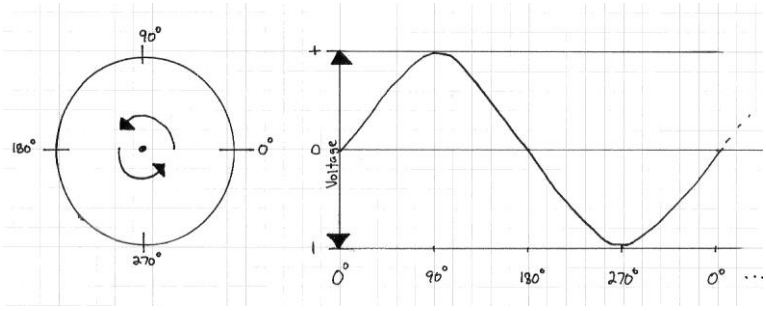


Fig. (1): Generation of AC voltages and currents



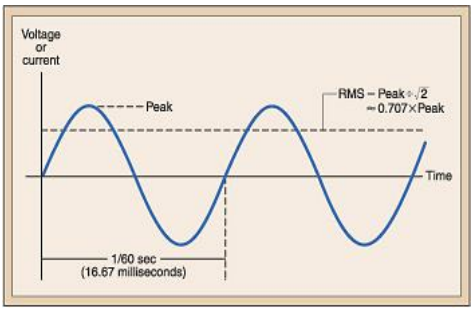


Fig. (2): Sine wave

Alternating quantity (voltage or current): AC voltage or current is defined as the alternating quantity which constantly changes in amplitude and whose direction reverses at regular intervals of time.

As shown in fig.(2), the amplitude of a sine wave increases from zero to a maximum in one direction, then falls to zero, reverses its direction, becomes maximum in opposite direction and then falls to zero again i.e., the wave changes its amplitude and direction with time. During the positive portion of voltage, the current flows in one direction and during the negative portion of voltage the current flows in the opposite direction. Both positive and negative portions are symmetrical.

Sine wave: An **alternating** quantity (current and voltage) obeys sine law; hence it is called a sinusoidal wave, referred as a Sine wave.

Some definitions of a Sine wave:

Cycle: The complete + Ve and – Ve portions of the sine wave are called one cycle.

Frequency (f): The number of cycles that a sine wave completes in one second is called

frequency. Unit hertz, Hz (s^{-1}).

Time Period (T): The time taken by the sine wave to complete one full cycle is called the Time Period. Unit second (s).

The sine wave equation:

A sine wave shown in fig.(2) is represented by the equations

$v = V_m \, Sin \, \omega t$ …… *for ac voltage*

$i = I_m \, Sin \, \omega t$ …… *for ac current*

Where V_m is the peak (maximum) value of the voltage and I_m is the peak (maximum) value of the current. *'v'* is the voltage at any instant of time called instantaneous value of voltage and *'i'* is the current at any instant of time called instantaneous value of current. ω is called the angular frequency and *'ωt'* is the phase angle of the sine wave.

Different forms of Sine wave equation.

$v = V_m \, Sin \, \theta$	$i = I_m \, Sin \, \theta$
$v = V_m \, Sin \, \omega t$	$i = I_m \, Sin \, \omega t$
$v = V_m \, Sin \, 2 \pi f t$	$i = I_m \, Sin \, 2 \pi f t$
$v = V_m \, Sin \, \frac{2\pi}{T} t$	$i = I_m \, Sin \, \frac{2\pi}{T} t$

Characteristics of a Sine wave:

a) Its one cycle spreads over 360^0
b) Its polarity reverses for every half cycle
c) It has maximum positive value at 90^0 and maximum negative value at 270^0
d) It has zero value at o^0, 180^0 and 360^0
e) It changes its value fastest when it crosses the zero axis
f) It changes its value the slowest when near its +ve maximum value and –ve maximum value.

Different values of sindusoidal voltage and current.

As the magnitude of the sine wave is not constant, thus the waveform can be measured in different ways. They are
(1) Instantaneous Value
(2) Average value
(3) Peak value
(4) Peak to peak value
(5) Amplitude
(6) Root Mean Square value (rms value)

Instantaneous Value:

The instantaneous value of an alternating voltage or current is the value voltage or current at any instant of time as shown in fig.(1). This value is different at different times along the waveform.

Average value:

The average value of an alternating voltage or current is the average of all instantaneous values during one half cycle (+ve or –ve).

(Note: The average value over a complete cycle is zero. Because the voltage is positive during one half cycle and negative during the other half cycle, therefore, the average value of the voltages occurring during the complete cycle is zero)

Root Mean Square value (RMS value):

An alternating voltage or current in circuits are generally stated as Root Mean Square values (RMS value) rather than by their maximum or peak values. The RMS values of voltage and current are represented by V_{rms} and I_{rms} respectively. RMS values are effective values.

Peak value:

It is the maximum value of an alternating voltage (V_p) or current (I_p) during +Ve or –Ve half cycle. The peak value applies to both +ve and –ve values of the cycle.

Peak to Peak value:

It is the **sum** of the +ve and –ve maximum values of an alternating voltage or current usually written as $V_{p\text{-}p}$ or $I_{p\text{-}p}$value.

During each complete cycle of a sine wave there are always two peak values, one for the positive half-cycle and the other for the negative half-cycle. This value is twice the peak value of a sine wave, i.e. the peak to peak value of the sine wave is the value from +ve to –ve peak as shown in fig.(1).

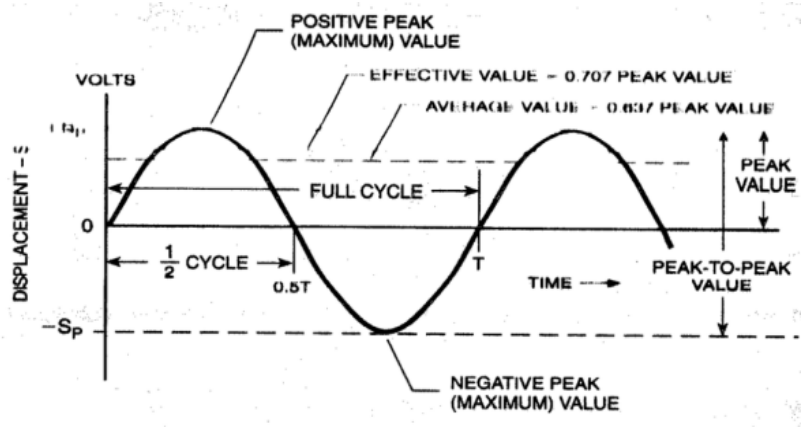


Fig.(1)

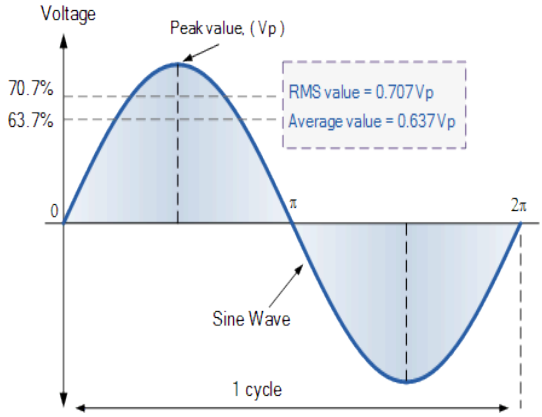
Expression for Average value:

Definition: It is defined as the "amount of AC power that transfers the same charge as is transferred by the DC power through the same resister for the same time". The symbols used for defining an Average value are V_{avg} **or** I_{avg}.

Let us consider a Sinusoidal current as $i = I_m \sin\theta$.

$$I_{av} = \frac{1}{\pi}\int_0^{\pi} i\,d\theta = \frac{1}{\pi}\int_0^{\pi} I_m \sin(\theta)\,d\theta = \frac{1}{\pi} I_m \left[-\cos(\theta)\right]_0^{\pi}$$

$$= \frac{1}{\pi} I_m (1 - (-1)) = \frac{2}{\pi} I_m = 0{,}637\, I_m$$



That is I_{avg} = 63.7% of the maximum value I_m of a sine wave. Similarly, V_{avg} = 63.7% of the maximum value V_m of a sine wave.

The Effective value or Root Mean Square (rms) value of a Sine wave:

The alternating voltage and current are expressed in Effective value rather than in peak-to-peak value. The effective value of a sine wave is computed by taking equally-spaced instantaneous values of current along the curve and extracting the square root of the average of the sum of the squared values. For this reason, the effective value is often called the "root-mean-square (rms)" value. Thus,

$$I_{eff} = \sqrt{\text{Average of the sum of the squares of } I_{inst.}}$$

Expression for RMS value of AC current:

Definition: It is defined as the "amount of AC power that produces the same heating effect as an equivalent DC power in a same resister for a same time". The symbols used for defining an RMS value are V_{RMS} or I_{RMS}

Let us consider a Sinusoidal current $i = I_m \sin\theta$.

$$I_{RMS}^2 = \frac{1}{2.\pi}\int_0^{2\pi} i^2 d\theta = \frac{1}{2.\pi}\int_0^{2\pi} I_m^2 \sin^2(\theta)\, d\theta = \frac{1}{2.\pi}\frac{I_m^2}{2}\int_0^{2\pi}(1 - \cos 2\theta).d\theta$$

$$= \frac{1}{2.\pi}\frac{I_m^2}{2}\left[\theta - \frac{1}{2}\sin(2\theta)\right]_0^{2\pi} = \frac{2.\pi}{2.\pi}\frac{I_m^2}{2} = \frac{I_m^2}{2}$$

$\sin(4.\pi)/2 - \sin(0)/2 = 0 - 0 = 0$

$$I_{RMS}^2 = \frac{I_m^2}{2} \qquad \text{Therefore } I_{RMS} = \sqrt{\frac{I_m^2}{2}} = 0{,}707\, I_m$$

Therefore, for the effective value or RMS value of AC current, I_{eff} or $I_{rms} = 0.707 \times I_m$

i.e., I_{rms} = 70.7% of the maximum value I_m of a sine wave.

Similarly, V_{rms} = 70.7% of the maximum value V_m of a sine wave.

Note: At this point it is found that a maximum ac value of 1.414 amperes is required in order to have the same heating effect as direct current. Therefore, in the ac circuit the maximum current required is 1.414 times the effective current.

Form Factor:

The form factor for a sin wave is defined as the ratio of R.M.S value to the Average value

$$\text{Form Factor of a sine wave} = \frac{\text{Root Mean Square value}}{\text{Average value}} = \frac{0{,}707\ \text{Maximum value}}{0{,}637\ \text{Maximum value}} = 1{,}11$$

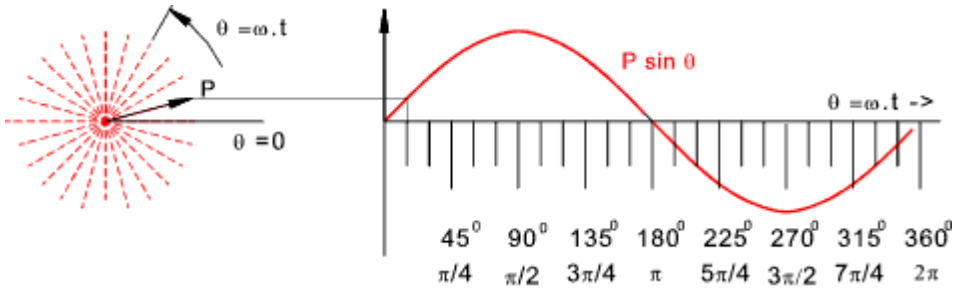
Peak or Crest Value:

The peak or crest value of a sine wave is defined as the ratio of Maximum value to the R.M.S value

$$\text{Peak /Crest value of a sine wave} = \frac{\text{Maximum value}}{\text{Root Mean Square value}} = \frac{\text{Maximum value}}{0{,}707\ \text{Maximum value}} = 1{,}414$$

Phaser (or) Vector Representation of sinusoidal waveforms :

A sinusoidal waveform can be shown as a plot of amplitude against time or $\theta = \omega.t$. In can also be shown as a rotating vector or phaser. Both these methods are illustrated below. Thus, Phasor can be used to represent sinusoidal waveforms.



The rotating vector on the left is assumed to be rotating at a constant angular velocity ω and its projection on the vertical axis = P sin ω t. = P sin θ is plotted as shown on the right.

Circuit Analysis using complex number representation and operator 'j'.

The amplitude and phase angle of sinusoidal waveforms can be written in the form of a complex number. Also many problems in AC circuits get simplified by the use of Operator 'j'.

Operator 'j' is used to represent an imaginary quantity of the complex number. Mathematically, it is given a value, i.e., j = $\sqrt{-1}$.

Significance of operator 'j' : When operator 'j 'is applied on a vector quantity $\overline{A}$ i.e., j $\overline{A}$, it denotes the rotation of the vector through 90^0 in anti-clockwise direction i.e., OX to OY in Fig.(1). Similarly, - j $\overline{A}$ denotes the rotation of the vector through 90^0 in the clock wise direction, i.e., OX to OY'. The double operation of j on a vector, rotates it in anti-clockwise direction through 180^0 i.e., from OX to OX'. Thus, j2 $\overline{A}$ = - $\overline{A}$.

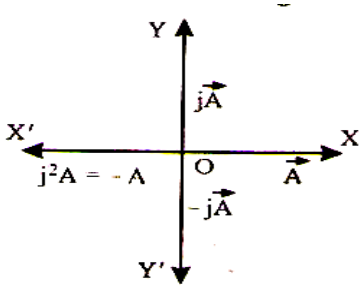


Fig.(1)

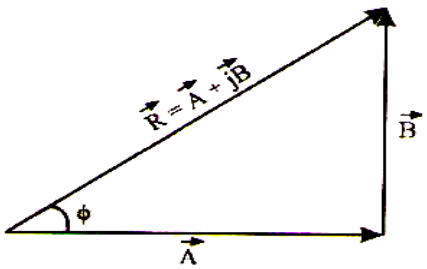


Fig.(2)

The combination of a real quantity $\overline{A}$ and an imaginary quantity $j\overline{B}$ is called a complex quantity. Thus the resultant

$$\bar{R} = \overline{A} + j\overline{B}$$

represents a complex quantity, where j $\overline{B}$ represents that the vector $\overline{B}$ is taken perpendicular to vector $\overline{A}$, shown in fig.(2).

The magnitude of the resultant vector $\overline{R}$ is given by $|R| = \sqrt{A^2 + B^2}$

and its direction (+Ve or anti clock wise, ccw) with respect to $\overline{A}$ is given by $\varphi = \tan^{-1} B/A$

Application of opeartor 'j' : To understand the application of opeartor j, consider that an AC voltage $v = V_m \, Sin \, \omega t$ is applied across an inductor L. Since the voltage across the inductor ($V_L = \omega LI_m$) leads the current I passing through it by 90^0, hence by the use of operator j, we may write $V_L = j \omega L I_m$, because multiplication by j means rotation by a +Ve angle of 90^0. Thus the inductive reactance (opposition to the flow of current by L) is $X_L = \omega L$ is completely given by the term j ω L.

Similarly, capacitive reactance (opposition to the flow of current by C) is $X_c = 1/\omega C$ is completely given by - j/ω C = 1/j ω C, because the voltage across the capacitor (V_C) lags the current I passing through it by 90^0.

If we have resistance R in series with an inductance L, then the impedance Z (total opposition to the current flow by L and R) is given by Z= R + j ω L ,

$$\text{its magnitude is } |Z| = \sqrt{R^2 + \omega^2 L^2}$$

$$\text{and phase angle } \emptyset = tan^{-1} \frac{\omega L}{R}$$

Similarly, vector impedance of R in series with C is given by

$$Z = R - \frac{j}{\omega C}$$

$$|Z| = \sqrt{R^2 + \frac{1}{\omega^2 C^2}} \quad \text{and } \emptyset = tan^{-1}\left(\frac{-1}{\omega CR}\right)$$

In the same way, Z of a circuit containing $R, L \, and \, C$ in series is given by

$$Z = R + J\,\omega L - \frac{1}{j\omega C}$$

$$= R + J\,(\omega L - \frac{1}{\omega C})$$

$$|Z| = \sqrt{R^2 + \left(\omega L - \frac{1}{\omega C}\right)^2}$$

and $$\emptyset = tan^{-1}\left[\frac{\left(\omega L - \frac{1}{\omega C}\right)}{R}\right]$$

Power factor:

Power is the rate of doing work and Power factor is the measure of Power how effectively utilized by the circuit. Power is designated by P and Power factor by Cos ∅, i.e., cosine of the angle between V and I in the circuit.

The power factor of a circuit can be defined in one of the following ways:

(i) Power factor (Cos ∅) is the cosine of angle between V and I in the circuit.

(ii) Power factor = $\frac{R}{Z} = \frac{\text{Resistance}}{\text{Impedance}}$

(iii) Power factor = $\frac{VI cos\,\emptyset}{VI} = \frac{\text{True power}}{\text{Apparent power}} = \frac{V_{avg}.I_{avg}}{V_{rms}.I_{rms}}$

It may be noted that power factor can never have a value greater than 1.

** Maximum value of Power factor ($Cos\emptyset$) is one only.

*** Power factor ($Cos\emptyset$) of the circuit, containing pure resistance is one (unity), because voltage and current are in phase in a pure resistance i.e ∅ = 0 and hence, $Cos\,\emptyset = 1$.

Significance of power factor:

The Power factor of a circuit is the measure of its effectiveness in utilizing the apparent power drawn by it. The greater the power factor, the greater is its ability to utilize the apparent power. For this reason, the power factor of a circuit should keep to unity.

Wattles current:

If the average power consumed in AC circuit is zero, the current in the circuit is said to be watt less current.

It is possible when the power factor is zero. i.e., when $Cos\emptyset = 0 \implies \emptyset = \frac{\pi}{2} = 90^0$

Thus, wattles current is possible when voltage and current are 90^0 out of phase. It is possible in case of a pure inductance/capacitance where the current lags/leads the voltage by 90^0.

Thus, in a pure inductance/capacitance, the average power consumed is zero.

R-L SERIES CIRCUIT:

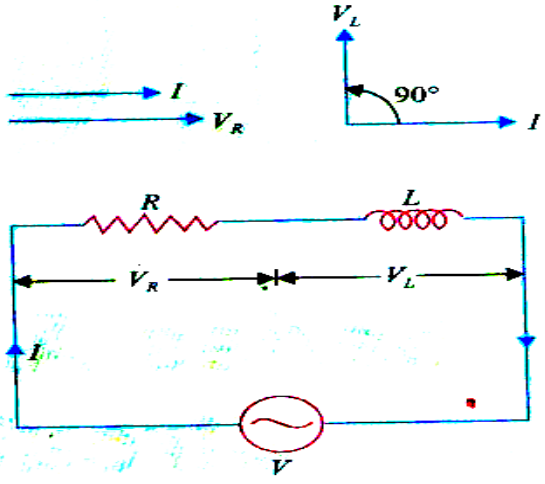
Fig. (1a) shows a pure resistance R ohm connected in series with a coil of pure inductance of L henry.

Let V = r.m.s. value of the applied voltage

I = r.m.s value of the circuit current

∴ V_R = IR…...where V_R is in phase with I

V_L= IX_L …where V_L leads I by 90^0



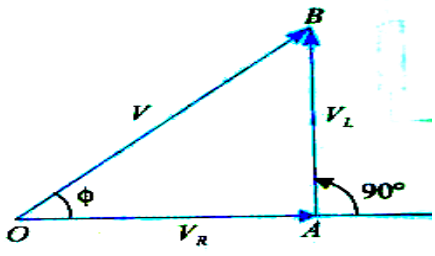


Fig.1(a) Fig.1(b)

Taking current as the reference phasor, the phasor diagram of the circuit can be drawn as shown in fig.(1b). The voltage drop V_R(= IR) is in phase with current and is represented in magnitude and direction by phasor OA. The voltage drop V_L ($=IX_L$) leads current by 90^0 and is represented in magnitude and direction by the phasor AB. The applied voltage V is the phasor sum of these two drops i.e.,

$$V = \sqrt{V_R^2 + V_L^2} = \sqrt{(IR)^2 + (IX_L)^2} = I\sqrt{R^2 + X_L^2}$$

$$\therefore \quad I = \frac{V}{\sqrt{R^2 + X_L^2}}$$

$\therefore$ $I = V/Z$ where $Z = \sqrt{R^2 + X_L^2}$

The quantity $\sqrt{R^2 + X_L^2}$ offers opposition to current flow and is called **Impedance** of the circuit. It is represented by Z and is measured in ohms (Ω).

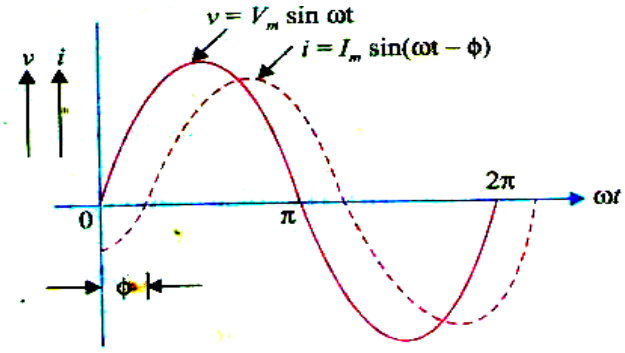


Fig.(2)

It is clear from the phasor diagram that circuit current I lags the applied voltage V by $\emptyset^o$. This is also shown in Fig. (2). The value of phase angle ∅ can be determined from the phasor diagram as: $\tan \emptyset = \frac{V_L}{V_R} = \frac{IX_L}{IR} = \frac{X_L}{R}$

Since X_L and R are known, the value of ∅ can be calculated.

If the applied voltage is $v = V_m \sin \omega t$, then equation for the circuit current will be:

$$i = I_m \sin(\omega t - \emptyset)$$

where $I_m = V_m/Z$; $\quad \emptyset = \tan^{-1} X_L/R$

R.C. SERIES CIRCUIT:

Fig. (1) Shows a resistance of R ohms connected in series with a capacitor of C farad.

Let V = r.m.s. value of the applied voltage

I = r.m.s value of the circuit current

V_R = IR…..where V_R is in phase with I

V_C= IX_C …where V_C lags I by 90^0

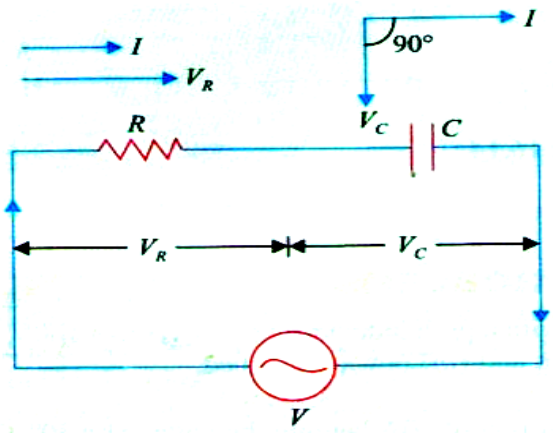


Fig.(1)

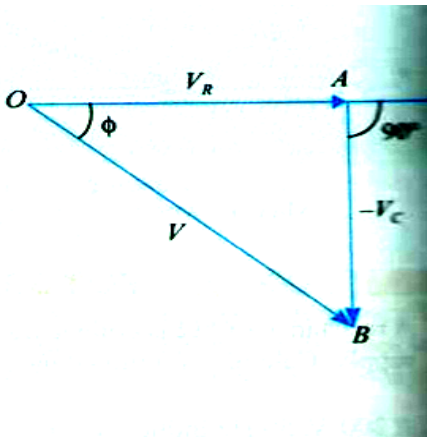


Fig. (2)

The phasor diagram of the circuit is shown in Fig.(2). The supply voltage V is the phasor sum of V_R (= IR) and V_C (= IX_C) drops i.e.

$$V = \sqrt{V_R^2 + V_C^2} = \sqrt{(IR)^2 + (-IX_C)^2} = I\sqrt{R^2 + X_C^2}$$

$$\therefore \quad I = \frac{V}{\sqrt{R^2 + X_C^2}}$$

The quantity $\sqrt{R^2 + X_C^2}$ offers opposition to current flow and is called **impedance** of the circuit.

$$\therefore \quad I = V/Z \text{ where } Z = \sqrt{R^2 + X_C^2}$$

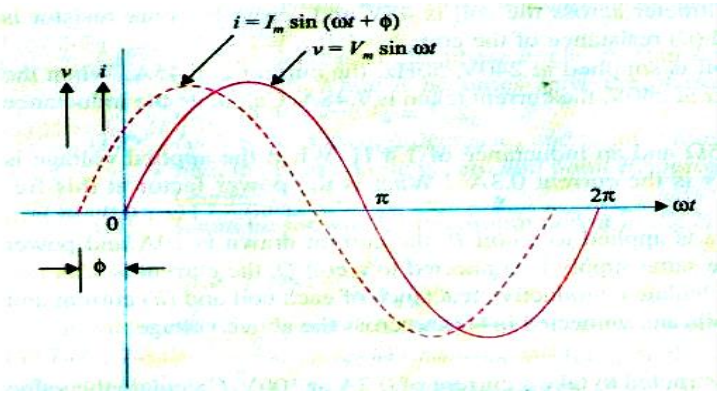


Fig. (3)

It is clear from the phasor diagram that circuit current I lead the applied voltage V by $\emptyset^o$.

Where: $\tan \emptyset = -\frac{V_C}{V_R} = -\frac{IX_C}{IR} = -\frac{X_C}{R}$

Since current is taken as the reference phasor, negative phase angle implies that voltage lags the current. This is the same thing as current leads the voltage See Fig. (3)).

R-L-C SERIES CIRCUIT:

This is a general series a.c. circuit. Fig.(1) shows R,L and C connected in series across a supply voltage V (r.m.s). The resulting circuit current is I (r.m.s).

∴ Voltage across R, V_R = IR … V_R is in phase with I

Voltage across L, V_L = IX_L …where V_L leads I by 90^0

Voltage across C, $V_C = IX_C$ …where V_C lags I by 90^0

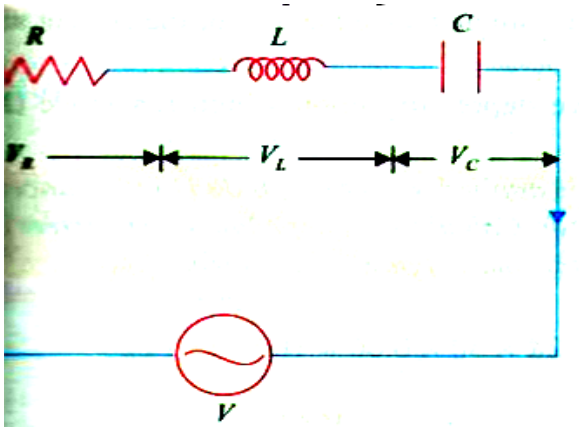


Fig.(1)

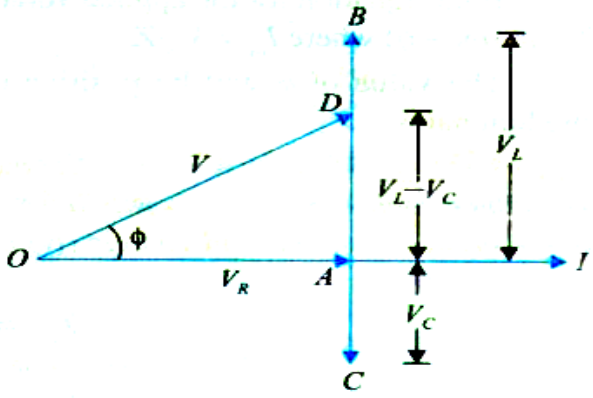


Fig.(2)

As before, phasor diagram is drawn taking current as the reference phasor. In the phasor diagram (See Fig. (2), OA represents V_R, AB represents V_L and AC represents V_C . It follows that the circuit can either be effectively inductive or capacitive depending upon which voltage drop (V_L or V_C) is predominant. For the case considered, $V_L > V_C$ so that net voltage drop across L-C combination is $V_L - V_C$ and is represented by AD. Therefore, the applied voltage V is the phasor sum of V_R and $(V_L - V_C)$ and is represented by OD.

$$V = \sqrt{V_R^2 + (V_L - V_C)^2}$$

$$= \sqrt{(IR)^2 + (IX_L - IX_C)^2} = I\sqrt{R^2 + (X_L - X_C)^2}$$

$$\therefore \quad I = \frac{V}{\sqrt{R^2 + (X_L - X_C)^2}}$$

The quantity $\sqrt{R^2 + (X_L - X_C)^2}$ offers opposition to current flow and is called **impedance** of the circuit.

Circuit power factor, $\cos \emptyset = \frac{R}{Z} = \frac{R}{\sqrt{R^2 + (X_L - X_C)^2}}$ → (1)

$$\tan \emptyset = \frac{V_L - V_C}{V_R} = \frac{X_L - X_C}{R} \quad \rightarrow (2)$$

Power consumed, $P = VI \cos \emptyset = I^2 R$

Three cases of R-L-C series circuit, we have seen that the impedance of a R-L-C series circuit is given by $Z = \sqrt{R^2 + (X_L - X_C)^2}$

(i) When $X_L - X_C$ is positive (i.e., $X_L > X_C$), the phase angle $\emptyset$ is positive and the circuit is inductive.

(ii) When $X_L - X_C$ is negative (i.e., $X_L > X_C$), the phase angle $\emptyset$ is negative and the circuit is capacitive.

(iii) When $X_L - X_C$ is zero (i.e., $X_L = X_C$), the phase angle $\emptyset$ is zero and the circuit is purely resistive

If the equation for the applied voltage is $v = V_m \sin \omega t$ then equation for the current will be:

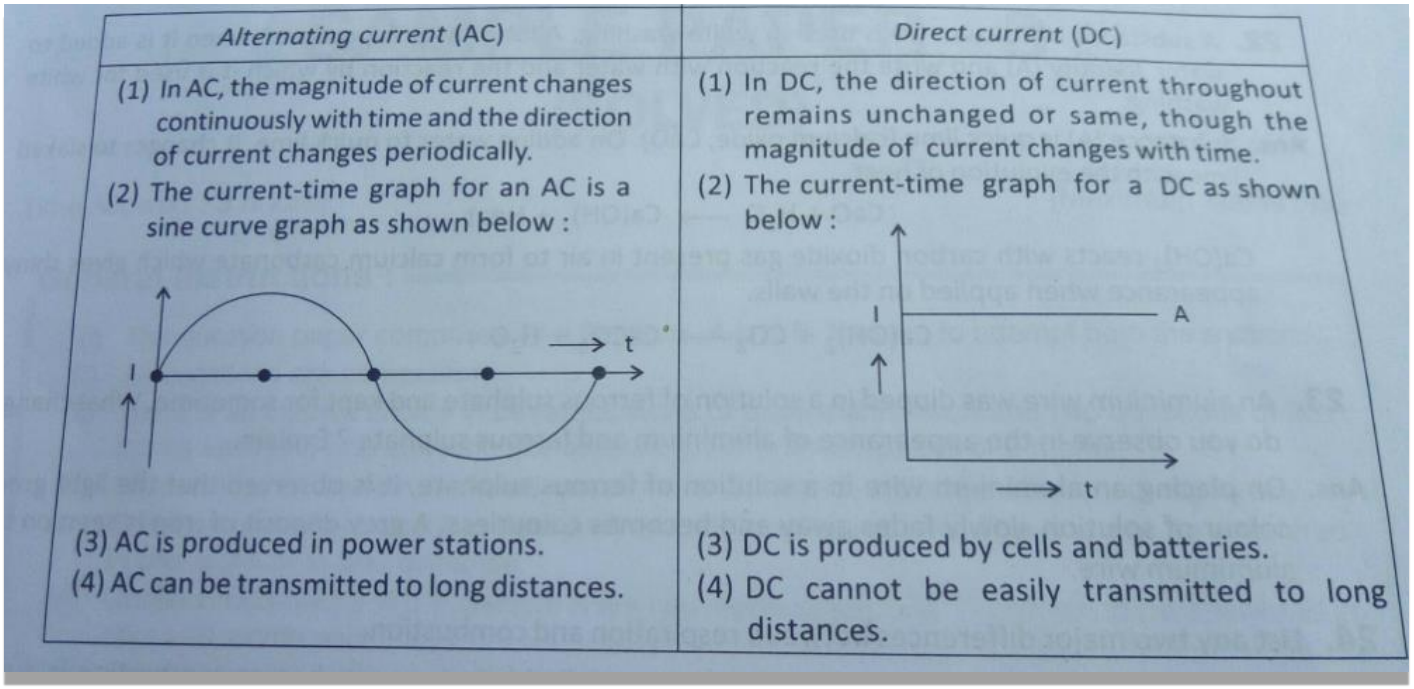
$i = I_m \sin(\omega t \pm \emptyset)$ where $I_m = V_m / Z$

The value of $\emptyset$ will be positive or negative depending upon which reactance (X_L *or* X_C) predominates.

The major differences between Alternating Current and Direct Current are given in the table below:

Alternating Current	**Direct Current**
AC is safe to transfer longer distance even between two cities and maintain the electric power.	DC cannot travel for a very long distance. It loses electric power.

The rotating magnets cause the change in direction of electric flow.	The steady magnetism makes DC flow in a single direction.
The frequency of AC is dependent upon the country. But generally, the frequency is 50 Hz or 60 Hz.	DC has no frequency. (Zero frequency).
In AC the flow of current changes its direction backwards periodically.	It flows in a single direction steadily.
Electrons in AC keep changing its directions – backward and forward	Electrons only move in one direction – that is forward.



PASSIVE FILTER CIRCUITS

Q. What is a filter circuit? What are its uses?

A passive filter circuit is a circuit which contain any combination of passive components R, L and C. These are frequently used in radio, T.V and other electronic circuits. Their purpose is

(i) To select the desire frequency from a complex input wave

(ii) To reject the undesired frequency

(iii)To apply only the desired frequency component to the circuit.

where it is required.

Q. What are different types of filter circuits?

There are four types of filters circuits.

(i) Low pass filter (ii) High pass filter (iii) Band pass filter (iv) Band stop filter. All these filter circuits made up of inductors and capacitors along with resistors which under ideal conditions are assumed to have no loss.

Q. Discuss the working of low pass filter and high pass R C filter circuits along with necessary theory?

High pass filter: High pass filter circuit is a circuit which passes high frequency (components) signals, but it attenuates low frequency signals.

The circuit of fig (1a) shows a basic C R high passes filter circuit. It transmits currents of all frequencies lying between certain frequency *fc* and infinity and all other frequencies are attenuated.

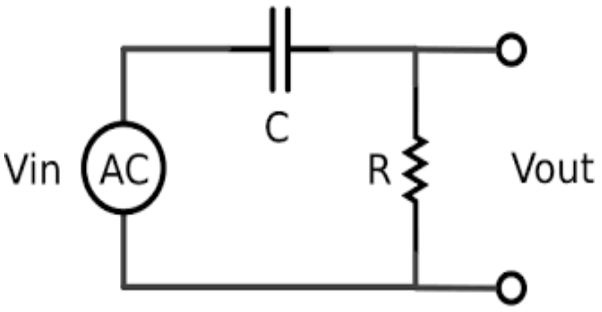


Fig.(1a)

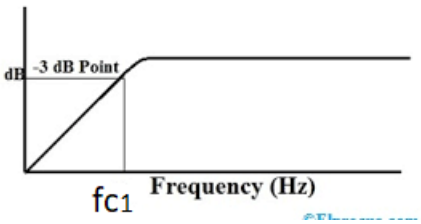


Fig.(1b)

Working principle: Since the reactance of the capacitor ($Xc = 1/\omega_c$) decreases with the increase in frequency and hence the higher frequency components in the input signal appear at the output with less attenuation than the low frequency components.

At extremely high frequencies, the reactance X_c is small and the capacitor 'C' acts almost as a short circuit and virtually all the input appears at the output. Thus, this circuit behaves as high pass filter circuit.

Frequency response curve: Frequency response curve of the CR high pass filter is shown in fig.(1b). For a sinusoidal input voltage V_i the output signal V_0 increases in amplitude with increasing the

frequency. The amplification factor or the gain of the circuit A and the angle θ by which the output leads the input are derived as follows.

From figure (1) we can write

$$V_O = \frac{R}{R + J\omega C} Vi$$

$$\therefore \quad A = \frac{V_O}{V_i} = \frac{R}{V_i(R + \frac{1}{J\omega C})} V_i = \frac{R}{R + \frac{1}{J\omega C}}$$

$$= \frac{1}{1 + \frac{1}{J\omega CR}} = \frac{1}{1 + \frac{1}{J2\pi fCR}} = \frac{1}{1 + \frac{f_{c_1}}{jf}}$$

$$\therefore \quad /A/ = \frac{1}{\sqrt{1 + (\frac{fc_1}{f})^2}} \quad \text{and} \quad \theta = Tan^{-1}(\frac{fc_1}{f})$$

Here $f_{c_1} = \frac{1}{2\pi Rc}$, is called lower cutoff frequency at which the magnitude of capacitive reactance is equal to the resistance and the gain is 70.7% of its maximum value. This frequency fc_1 is also called as the lower 3db frequency.

R C low pass filter circuit:

The circuit of fig (2a) shows low pass R C filter circuit. It transmits the currents of all frequencies lying between '0' to a certain frequency called cutoff frequency f_C and all other frequencies above the cutoff frequency are attenuated.

The circuit of the low pass filter circuit is shown in fig (2) is identical with the high pass filter circuit except that the output is now taken across the capacitor instead of the resistor 'R'.

Working: Since the reactance of the capacitor 'C' decreases with the increase in frequency, this circuit passes low frequencies but attenuates high frequencies. At extremely high frequencies the capacitor acts as a virtual short circuit and the output falls to zero.

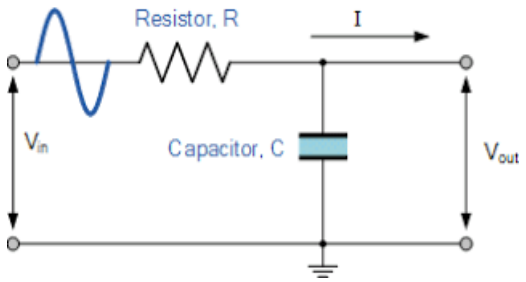


Fig. (2a)

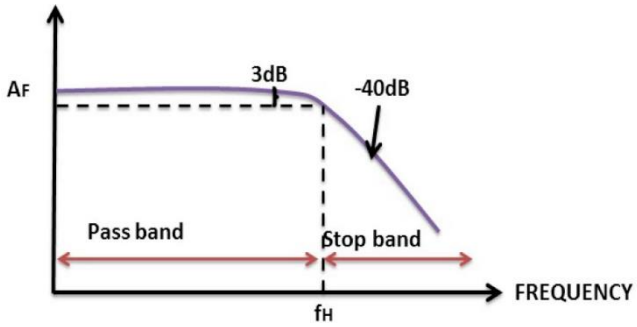


Fig. (2b)

Frequency response curve: Frequency response curve of the RC lowpass filter is shown in fig.(2b). For a sinusoidal input voltage Vi, the output signal voltage Vo decreases in amplitude with the increase in frequency. The frequency response curve is shown in fig (2.b). For the circuit shown in

fig (2a), the magnitude of the gain 'A' and the angle θ by which the output voltage leads the input are derived as follows.

From fig (2a) we can write

$$Vo = \frac{Vi\dfrac{1}{J\omega C}}{R+\dfrac{1}{J\omega C}}$$

$$\therefore \quad \text{Gain} \quad A = \frac{Vo}{Vi} = \frac{Vi\dfrac{1}{J\omega C}}{(R+\dfrac{1}{J\omega C})Vi} = \frac{\dfrac{1}{J\omega C}}{R+\dfrac{1}{J\omega C}} = \frac{1}{1+J\omega CR}$$

$$= \frac{1}{1+JRC2\pi f} = \frac{1}{1+J\dfrac{f}{f_{C_2}}}$$

$$\therefore \quad /A/ = \sqrt{1+\left(\frac{f}{f_{c2}}\right)^2} \quad \text{and} \quad \theta = tan^{-1}\left(\frac{f}{f_{c2}}\right)$$

where $f_{C_2} = \dfrac{1}{2\pi RC}$, Here f_{C_2} is called upper 3db frequency at which the gain falls to 70.7% value of its maximum value. At this frequency, the capacitive reactance is equal to the resistance.

RL high pass filter: The basic RL high pass filter is shown in fig (1a). It transmits currents of all frequencies lying between a certain frequency, called cutoff frequency, f_C and infinity and all other frequencies below the cutoff frequency are attenuated.

Working: Since the reactance of the inductor 'L' increases with the increase in frequency, so high frequency signals in the input signal appear at the output with less attenuation than do the low frequency components. At low frequencies, the inductive reactance is so small and most of the input voltage by passes through the inductor. Thus, the circuit passes high frequency components readily but attenuates low frequencies. Thus, the circuit acts as a high pass filter circuit.

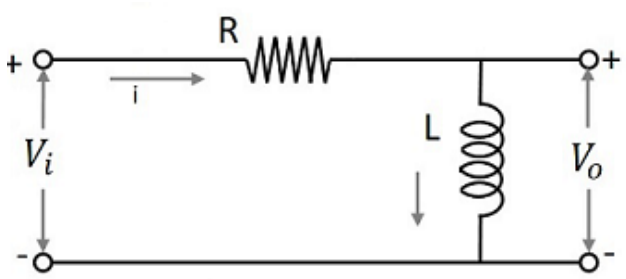


Fig. (1a)

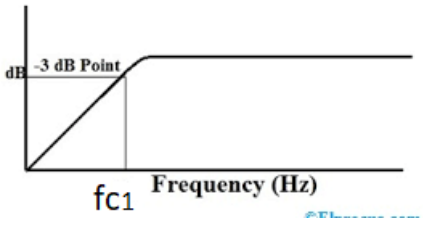


Fig.(1b)

Frequency response curve: Fig (1b) shows the frequency response curve. For a sinusoidal input voltage V_i, the output voltage V_O increases in amplitude with the increase in frequency. The magnitude of the gain A and the angle θ by which the output voltage leads the input voltage are derived as follows.

From fig (2), we can write the output voltage.

$$V_O = V_i \frac{J\omega L}{R + J\omega L}$$

$$\therefore \quad A = \frac{V_O}{Vi} = \frac{J\omega L}{R + J\omega L} = \frac{1}{1 + \frac{R}{J\omega L}} = \frac{1}{1 + \frac{R}{J2\pi fL}}$$

$$= \frac{1}{1 + \frac{f_{C_1}}{Jf}} = \frac{1}{1 + \frac{f_{C_1}}{Jf}} \quad \text{where} \quad f_{C_1} = \frac{R}{2\pi L}$$

$$\therefore \quad /A/ = \frac{1}{\sqrt{1 + (\frac{f_{C_1}}{f})^2}} \quad \text{and} \quad \theta = Tan^{-1}(\frac{f_{C_1}}{f})$$

The frequency f_{C_1} is called lower cutoff frequency or lower 3db frequency at which the gain is equal to 70.7% of maximum value. At this frequency, the magnitude of the X_L is equal to the resistance.

Q. Discuss the working of LR low pass and high pass filters with necessary theory?

Low pass filter: The circuit fig (2a) shows a basic R L low pass filter circuit. It transmits currents of all frequencies between zero to a certain frequency; called cutoff frequency and all other frequencies above the cutoff frequency are attenuated.

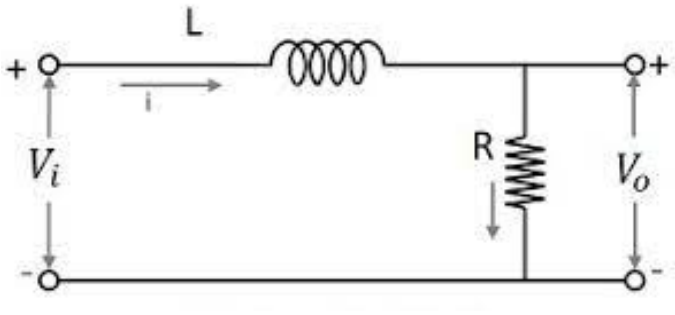


Fig.(2a)

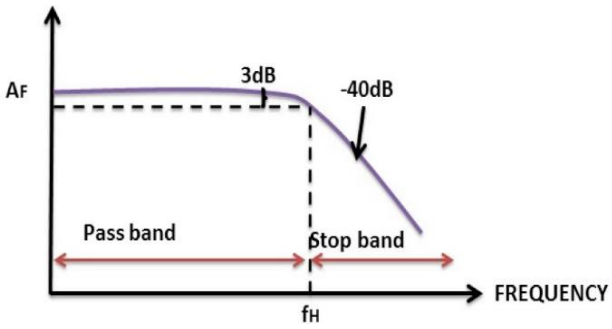


Fig.(2b)

Since inductive reactance X_L increases with the increase in frequency, so high frequency components in the input may appear across the inductor whereas the low frequency components appear at the output. Since X_L is small for low frequencies, at low frequencies the inductor acts almost as a short circuit and virtually all the input voltage appears at the output. At high frequencies, the inductive reactance is infinite and hence behaves as an open circuit. Thus, input voltage cannot reach the output terminals. Thus, the circuit acts as low pass filter.

Frequency response curve: Fig. (2b) shows the frequency response curve. For a sinusoidal input voltage V_i , the output signal V_o decreases in amplitude with increase in frequency. The amplification

factor or the gain 'A' of the circuit shown in fig (2a) and angle θ by which the output leads the input are derived as follows.

From fig (i) we can write the output voltage $Vo = Vi\dfrac{R}{R + J\omega L}$

$$\therefore \text{ Gain A} = \frac{V_o}{V_i} = \frac{V_i R}{(R + J\omega L)V_i} = \frac{R}{R + J\omega L}$$

$$= \frac{1}{1 + \dfrac{J\omega L}{R}} = \frac{1}{1 + \dfrac{J2\pi fL}{R}} = \frac{1}{1 + \dfrac{Jf}{f_{C_2}}}$$

$$\therefore \quad /A/ \quad = \sqrt{1 + \left(\frac{f}{f_{c2}}\right)^2} \qquad \text{and} \qquad \theta = tan^{-1}\left(\frac{f}{f_{c2}}\right)$$

Where $f_{C_2} = \dfrac{R}{2\pi L}$ is called the upper cutoff frequency at which the magnitude of the X_L is equal to R and the gain is equal to 70.7% of its maximum value. This frequency is also called as upper 3db frequency.

RC high pass filter as a differentiator:

Differentiating circuit: A circuit in which output voltage is directly proportional to the derivative of the input voltage is known as a differentiating circuit.

i.e. $V_O \alpha \dfrac{d}{dt}(iput)$

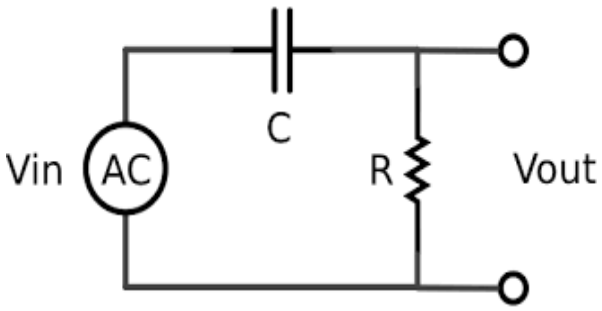


Fig (1) shows the typical differentiating circuit in which the output voltage across 'R' will be the derivative of the input voltage.

Let V_i be the input voltage and 'i 'be the resulting current. The charge on the capacitor at any instant is $q = CV_c$

Differentiating w.r t time, $\dfrac{dq}{dt} = C\dfrac{dV_c}{dt}$

$$i = C\frac{dV_c}{dt} \rightarrow (1)$$

Since the capacitor reactance ($X_C \rangle\rangle R$) is very larger than R, the input voltage can be considered equal to the capacitor voltage with negligible error.

i.e. $V_C = V_i$

But we taking the output voltage across the resistor, therefore the output voltage,

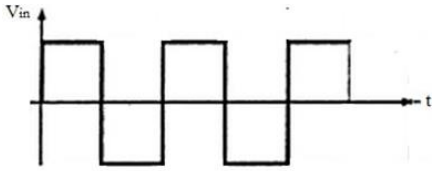
$$V_O = iR = RC\frac{d}{dt}(V_i) \qquad \text{from eqn. (1) and } V_C = V_i$$

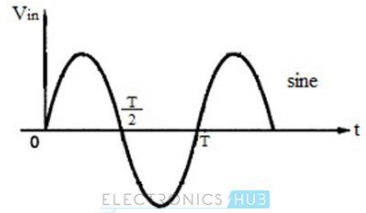
$$V_O \alpha \frac{d}{dt}(V_i) \qquad (\because RC = \text{time constant is constant})$$

Hence a high pass filter with a small (RC) time constant behaves like a differentiator.

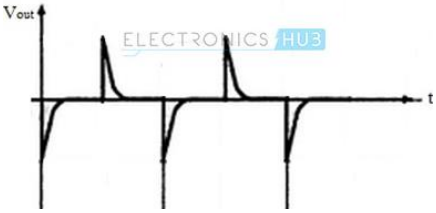
Waves forms:

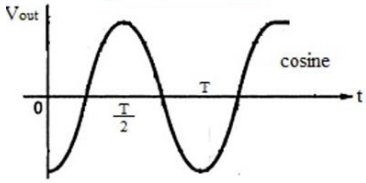
Input wave





Output wave

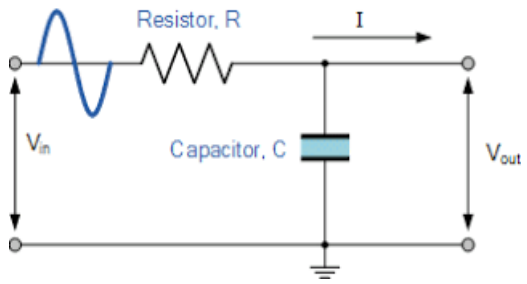




RC low pass filter as an integrating circuit:

A circuit in which output voltage is directly proportional to the integral of the input voltage is known as integrating Circuit. i.e., $V_o \alpha \int input$

Fig (1) shows a typical integrating circuit in which output voltage across the capacitor will be the integral of the input voltage



$$V_0 \propto \int V_i \, dt$$

Let V_i be the input voltage and "i" be the resulting current. Since R is large compared to capacitive reactance X_C of the capacitor, the input voltage can be considered equal to the voltage across 'R' with negligible error.

$$\text{i.e. } V_i = iR$$

$$\Longrightarrow \quad i = \frac{V_i}{R}$$

The charge on the capacitor at any instant is $q = \int idt$ $\left\{since \ \frac{dq}{dt} = i, \ q = \int idt\right\}$

Therefore, output voltage $V_O = \frac{q}{C} = \int \frac{idt}{C} = \frac{1}{C}\int \frac{V_i}{R} dt = \frac{1}{RC}\int V_i dt$

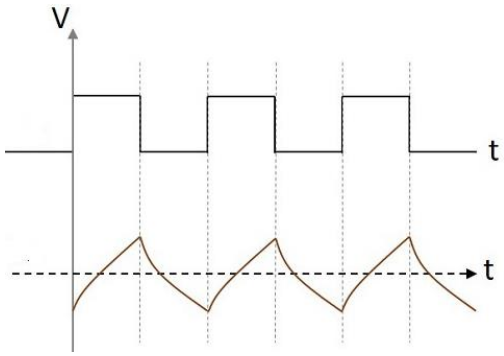
or $V_O \alpha \int input$ voltage

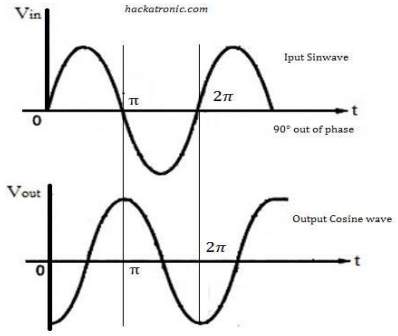
Hence low pass filter with large time constant (RC) behaves like an integrating circuit.

Wave forms:

Input wave

Output wave

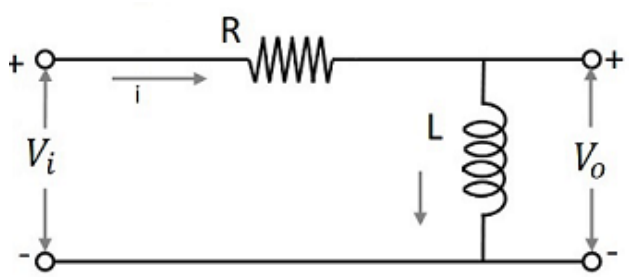




RL high pass filter as a differentiating circuit:

Differentiating circuit: A circuit in which output voltage is directly proportional to the derivative of the input voltage is known as a differentiating circuit. i.e., $V_O \alpha \int \frac{d}{dt}(input)$.

Fig (1) shows the typical differentiator circuit in which the output voltage across the inductor will be the derivative of the input voltage.



$V_O \alpha \int \frac{d}{dt}(input)$

Let Vi be the input voltage and 'i' be the resulting current. Since R is very large compared to inductive reactance X_L of the inductor and hence the input voltage can be considered as equal to the voltage across R with negligible error.

$$\text{i.e.} \quad V_i = Ri$$

$$\text{or} \quad i = \frac{V_i}{R}$$

Now the output voltage across the inductor is given by,

$$V_O = L\frac{di}{dt}$$

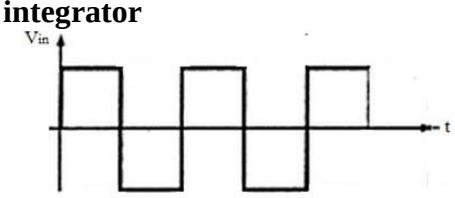
$$= L\frac{d}{dt}(\frac{V_i}{R}) = \frac{L}{R}\frac{d}{dt}(V_i) \qquad \because (i = \frac{V_i}{R})$$

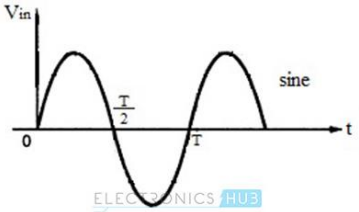
Therefore, $V_O \alpha \frac{d}{dt}(V_i)$ (since $\frac{L}{R}$ is a const. called time const.)

Thus, the output voltage of a high pass filter with small time constant is proportional to the derivative of the input voltage and hence it is known as differentiating circuit.

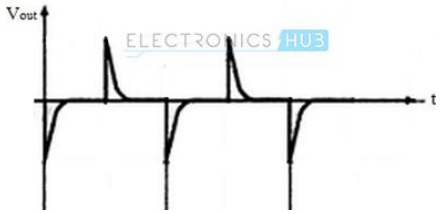
Wave forms of the integrator

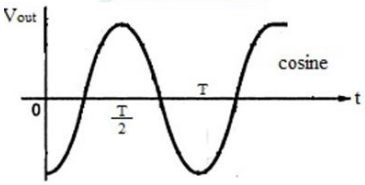
Input wave





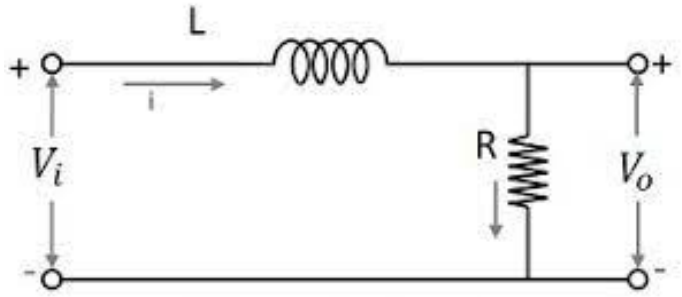
Output wave





LR low pass filter as an integrating circuit: A circuit in which output voltage is directly proportional to the integral of the input voltage is known as integrating Circuit. i.e. $V_o \alpha \int input$.

Fig (1) shows a typical integrating circuit in which output voltage across the resistor will be the integral of the input voltage.



$V_o \alpha \int input$

Let V_i be the input voltage and $'i'$ be the resulting current. Since the inductive reactance $X_L (X_L \rangle\rangle R)$ is very much larger than 'R', the input voltage can be considered equal to the voltage across 'L' with negligible error.

$$\text{i.e. } V_i = L\frac{di}{dt}$$

$$\text{or } \quad di = \frac{V_i}{L}dt$$

$$\text{or } i = \frac{1}{L}\int V_i dt$$

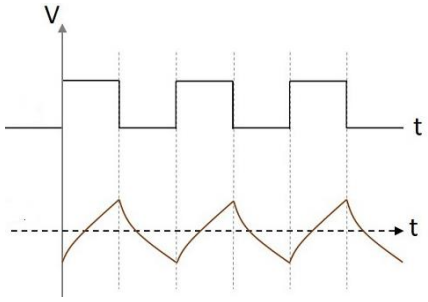
Now output voltage, $V_0 = iR = R\frac{1}{L}\int V_i dt$

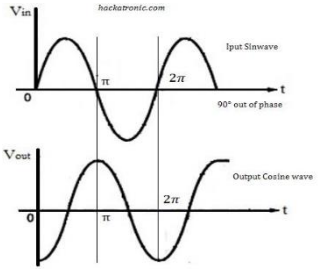
$V_O \alpha \int V_i dt$ Where $\frac{L}{R}$ is a const. called time constant of the circuit.

Hence a low pass filter with large time constant behaves like a integrating circuit.

Input wave form

output wave form





I B.Sc.,(CBCS),I-Sem. Unit-V: Resonance

RLC Series Resonance: *RLC Series resonance circuit, resonant frequency, Q-factor- bandwidth –Selectivity.*
RLC parallel Resonance: *RLC **P**arallel resonance circuit, resonant frequency, Q-factor- bandwidth –Selectivity.*
(Importance of Q-factor, Band width, Selectivity and their real time applications and usage)

Introduction to Resonance in ac circuits:

A circuit is said to be at resonance, when the frequency of an AC voltage applied, equals to the natural frequency of the circuit.

In a.c. circuits, however, the voltage and currents are usually out phase. Under certain conditions the current and voltage may be ***in phase*** and the circuit behaves as a ***pure resistive***. This phenomenon is known as ***resonance***. The resonance usually occurs at a single frequency, known as ***resonant frequency***.

In RLC series circuit the resonance occurs when the inductive reactance and capacitive reactance are equal in magnitude but cancel each other, where as in parallel RLC circuit the resonance occurs when inductive suceptance and capacitive susceptance are equal in magnitude, but cancel to each other.

Accordingly, there are two types of resonance in ac circuits, namely**, *series and parallel resonance.*** When the circuit is at resonance, the voltage applied and the current in the circuit are in phase, because they are 180 degrees apart in phase at resonance, and cancel each other. Hence the ***power factor*** of the circuit is ***unity*** at resonance.

Series resonance:

In RLC series circuit the resonance occurs when the inductive reactance and capacitive reactance are equal in magnitude but cancel each other, because they are 180 degrees apart in phase at resonance.

Applications of Series Resonance circuits:

Series Resonance circuits are one of the most important circuits used in electrical and electronic circuits. They are,

1. AC mains filters,
2. Noise filters and
3. Radio and Television tuning circuits (producing a very selective tuning circuit for the receiving of the different frequency channels).

Expression for the Resonant Frequency:

[Q. **Derive an expression for the resonant frequency of series LCR series resonant Circuit.]**

Fig (1) shows the LCR series resonant circuit. In it the resistance R, inductance L and capacitance C are connected in series with a source of e.m.f. $V = V_O Sin\omega t$ .The resistance 'R' includes the resistance of the inductor and the resistance of the source or Generator.

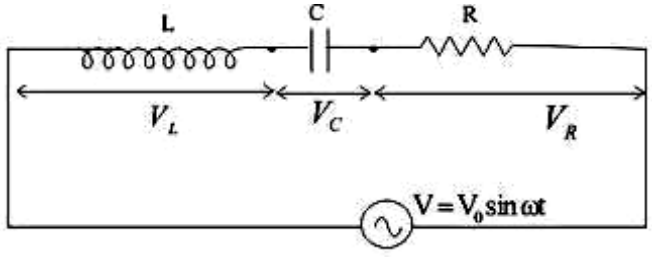


Fig (1) LCR series resonant circuit

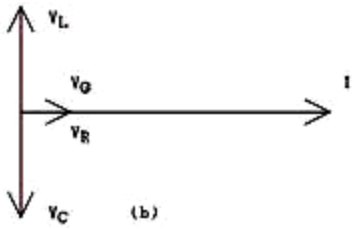


fig.(2) Vector diagram at resonance

The impedance of the circuit is given by $Z = R + J\omega L + \frac{1}{J\omega C} = R + J\omega L - \frac{J}{\omega c}$

$= R + J(\omega L - \frac{1}{\omega C})$ $\rightarrow$ eqn.(1)

At resonance, ω=ω0, the reactance component of the impedance is zero, i.e. $\omega_O L - \frac{1}{\omega_O C} = 0$

$$\text{or} \quad \omega_O L = \frac{1}{\omega_O C}$$

$$\text{or} \quad \omega_O{}^2 = \frac{1}{LC}$$

$$\text{or} \quad \omega_O = \pm\frac{1}{\sqrt{LC}}$$

Therefore, the resonant frequency, $f_r = \frac{1}{2\pi\sqrt{LC}}$ [since $\omega_0 = 2\pi f_r$]

At this frequency, the reactive term that varies with frequency disappear and /Z/ = R (from eqn.(1)). Thus at resonance, the impedance equals to R, while at any other frequency, the magnitude of the impedance Z is /Z/ = $\sqrt{R^2 + (\omega L - \frac{1}{\omega C})^2}$, which is always greater than R. Hence in series a RLC circuit at resonance the impedance is minimum and the current will be maximum and is given by $i_r = \frac{V}{R}$

Frequency response or Resonance curve:

The curve drawn between the current and frequency is called frequency response curve or resonance curve. As the frequency of the applied voltage is increased the current 'I' in the circuit varies as shown in fig (1).

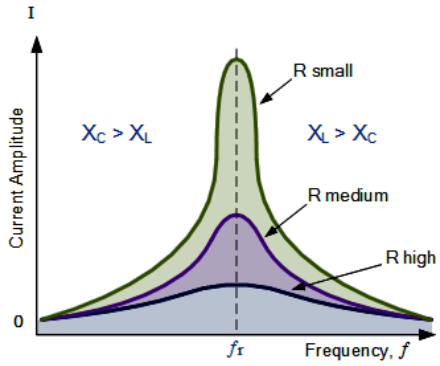


Figure.(1)

For smaller value of 'R' the curve is sharply peaked and for a larger value it is flat. The current is maximum at the resonant frequency, f_r and equal to $\frac{V}{R}$ amp. For frequencies less than f_r, ($X_L \langle X_C$) and therefore the circuit behaves like an RC circuit. And for frequencies greater than f_r, $X_L \rangle X_C$ and the circuit behaves like an RL circuit.

Bandwidth of a series resonance circuit:

The band width (BW) of a series resonance circuit is defined as "the range of frequencies over which current equals to or greater than 70.7% of its maximum value of current at resonance".

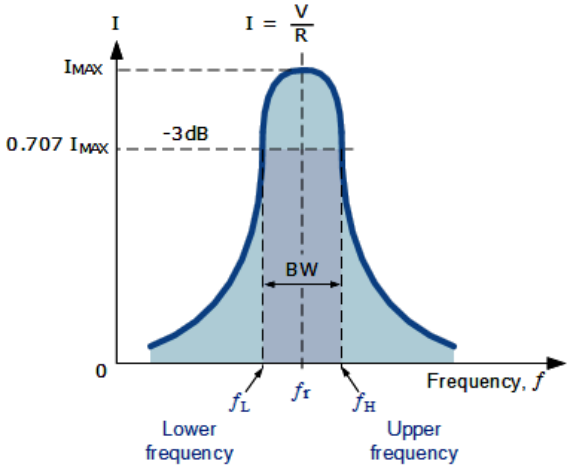


Figure.(1) frequency response curve of series RLC circuit.

In fig (1) $f_L and f_H$ are called *half power* or *-3dB* frequencies (taking 0dB as the maximum current reference) at which current is exactly equal to 70.7% of the maximum value . The frequency f_L is called lower cutoff frequency (lower half power frequency) and the frequency f_H is called the upper cutoff frequency (upper half power frequency). The distance between these two points, i.e. ($f_H - f_L$) is called the **Bandwidth**, (BW). The series resonance circuit offers low impedance in this frequency range.

Quality factor of a series RLC resonant circuit:

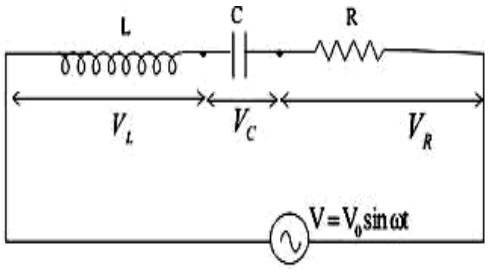
For a series RLC circuit it is defined as "the ratio of the voltage across either a capacitor, VC or an inductor, V_L to the supply voltage, V". So, it is simply as the voltage magnification.

At resonance, current is maximum i.e $i_r = \frac{V}{R}$.

Voltage across either 'C' or 'L' = $i_r X_L = i_r X_C$

Supply voltage V = $i_r R$

$\therefore$ Q-factor = $\frac{V_L}{V} = \frac{i_r X_L}{i_r R} = \frac{\omega_r L}{R} = \frac{2\pi . f_r L}{R}$.



Now, for series resonance, $f_r = \frac{1}{2\pi\sqrt{LC}}$.

$\therefore$ Q-factor = $\frac{2\pi L}{R}\frac{1}{2\pi\sqrt{LC}} = \frac{1}{R}\sqrt{\frac{L}{C}}$.

Similarly we can show that $Q\ factor = \frac{V_C}{V} = \frac{1}{R}\sqrt{\frac{L}{C}}$.

From the above equations V_L *or* V_c = *Q-factor x V.*

Since Q >1, therefore the circuit exhibits voltage magnification. For a series resonance circuit higher Q factor means higher is the sharpness of the resonance.

Pro.1.In series RLC circuit=100 ohm L=0.5 H and C = 40 μF. Calculate the resonant, lower and upper half power frequencies.

Solution: Resonant frequency, $f_o = \frac{1}{2\pi\sqrt{LC}}$

$= \frac{1}{2\times 3.14\sqrt{0.5\times 40\times 10^{-6}}} = \frac{1}{6.28\sqrt{20\times 10^{-6}}} = \frac{1}{6.28\times 10^{-3}\times 4.47}$ =35.6Hz

Lower half frequency, $f_1 = f_o - \frac{R}{4\pi L}$ =35.6 - $\frac{100}{4\times 3.14\times 0.5} = 35.6 - 15.9 = 19.7Hz$

Upper half power frequency, $f_2 = f_o + \frac{R}{4\pi L} = 35.6 + 15.9 = 51.5Hz$

Pro.2.In series LCR circuit the resonant frequency is 800 Hz. The half power points are obtained at frequencies 745 Hz and 855Hz. Calculate the value of Q.

Sol: Given, lower half power frequency =745Hz

upper half power frequency =855Hz

resonant frequency f_o =800 Hz

$$Q = \frac{f_o}{\Delta f} = \frac{f_o}{f_2 - f_1} = \frac{800}{855 - 745} = \frac{800}{110} = 7.3$$

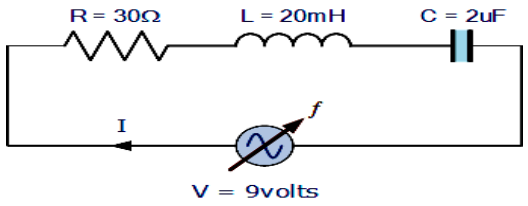
Prob.3: A series LCR resonance circuit has Q = 120 at resonance, a capacitance 200pF connected in series with an inductance of 150μH.Calculate its bandwidth?

Sol: Resonant frequency

$$f_o = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{6.28\sqrt{150\times 10^{-6}}\times 200\times 1o^{-12}} = 9.19\times 10^5\, Hz$$

Now Q-factor $= \frac{f_o}{f_2 - f_1} \Rightarrow \Delta f = \frac{f_o}{Q} = \frac{1}{120} 9.19\times 10^5 = 7.66kHz$

Prob.4: A series resonance network consisting of a resistor of 30Ω, a capacitor of 2uF and an inductor of 20mH is connected across a sinusoidal supply voltage which has a constant output of 9 volts at all frequencies. Calculate, the resonant frequency, the current at resonance, the voltage across the inductor and capacitor at resonance, the quality factor and the bandwidth of the circuit. Also sketch the corresponding current waveform for all frequencies.



Resonant Frequency, f_r

$$f_r = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{0.02\times 2\times 10^{-6}}} = 796Hz$$

Circuit Current at Resonance, I_m

$$I = \frac{V}{R} = \frac{9}{30} = 0.3A \text{ or } 300mA$$

Inductive Reactance at Resonance, X_L

$$X_L = 2\pi f L = 2\pi\times 796\times 0.02 = 100\Omega$$

Voltages across the inductor and the capacitor, V_L, V_C

$$V_L = V_C$$
$$V_L = I \times X_L = 300mA \times 100\Omega$$
$$V_L = 30volts$$

(Note: the supply voltage is only 9 volts, but at resonance the reactive voltages are 30 volts peak!)

Quality factor, Q

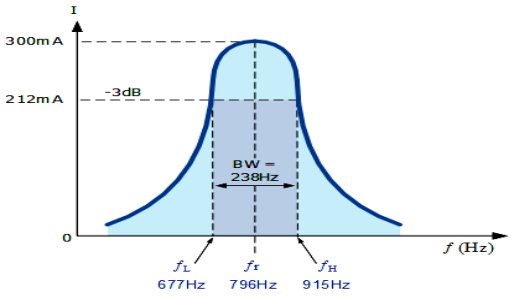
$$Q = \frac{X_L}{R} = \frac{100}{30} = 3.33$$

$$BW = \frac{f_r}{Q} = \frac{796}{3.33} = 238Hz$$

The upper and lower -3dB frequency points, f_H and f_L

$$f_L = f_r - \frac{1}{2}BW = 796 - \frac{1}{2}(238) = 677Hz$$

$$f_H = f_r + \frac{1}{2}BW = 796 + \frac{1}{2}(238) = 915Hz$$



Prob.5: A series circuit consists of a resistance of 4Ω, an inductance of 500mH and a variable capacitance connected across a 100V, 50Hz supply. Calculate the capacitance require to give series resonance and the voltages generated across both the inductor and the capacitor.

Resonant Frequency, f_r

$$X_L = 2\pi f L = 2\pi \times 50 \times 0.5 = 157.1\Omega$$

at resonance: $X_C = X_L = 157.1\Omega$

$$\therefore C = \frac{1}{2\pi f X_C} = \frac{1}{2\pi.50.157.1} = 20.3\mu F$$

Voltages across the inductor and the capacitor, V_L, V_C

$$I_S = \frac{V}{R} = \frac{100}{4} = 25Amps$$

at resonance: $V_L = V_C$

$$V_L = I \times X_L = 25 \times 157.1$$
$$\therefore V_L = 3{,}927.5volts$$

Problem 6: Find the value of inductance which should be connected in series with a capacitor of 5μF and resistor of 100Ω and an A.C. source of 50 c/s so that power factor of the circuit is unity.
Sol: The power factor of series LCR circuit is unity at resonance at which.
Inductive reactance = Capacitive reactance

$$\omega L = \frac{1}{\omega L}$$

$$\Rightarrow L = \frac{1}{\omega^2 C} = \frac{1}{(2\pi f)^2 C} = \frac{1}{4\pi^2 f^2 C} = \frac{1}{4\times(3.14)^2\times(50)^2\times5\times10^{-6}} = \frac{1}{4\times9.86\times2500\times5}$$

$$= 2.03\text{Henry}$$

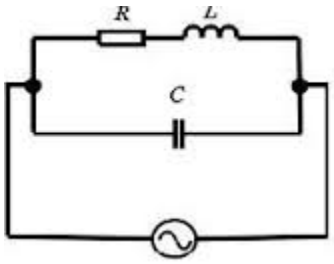
$$\therefore L = 2.03 Henry$$

Parallel resonance in RLC Circuits:

[Q. Draw the parallel resonance circuit and obtain an expression for its resonant frequency]

Fig (1) shows a parallel resonant circuit in which one branch consists of an inductance 'L' with associated resistance 'R' and other branch with a capacitance 'C' The resistance associated with capacitor is assumed to be negligible. An a. c. source of e m f E = $Eo \sin \omega t$ is connected across this parallel circuit.

The admittance (Y=1/Z) of the parallel circuit is given by,



$$Y = \frac{1}{Z} = \frac{1}{R + J\omega L} + \frac{1}{\frac{1}{J\omega C}} = \frac{1}{R + J\omega L} + J\omega C$$

$$= \frac{(R - J\omega L)}{(R + J\omega L)(R - J\omega L)} + J\omega C$$

$$= \frac{R}{R^2 + \omega^2 L^2} - J\left(\frac{\omega L}{R^2 + \omega^2 L^2} - \omega C\right) \rightarrow (1)$$

Fig.(1)

At resonance, the susceptive component of admittance is zero and $\omega = \omega_r$

$$\therefore \quad \frac{\omega_r L}{R^2 + \omega_r{}^2 L^2} - \omega_r C = 0$$

$$\text{or} \quad \frac{\omega_r L}{R^2 + \omega_r{}^2 L} = \omega_r C$$

$$\text{or} \quad R^2 + \omega_r{}^2 L^2 = \frac{L}{C} \qquad \rightarrow (2)$$

$$\text{or} \quad \omega_r{}^2 L^2 = \frac{L}{C} - R^2$$

$$\text{or} \quad \omega_r{}^2 = \frac{1}{LC} - \left(\frac{R}{L}\right)^2$$

$$\text{or} \quad f_r = \frac{1}{2\pi}\sqrt{\frac{1}{LC} - \left(\frac{R}{L}\right)^2}$$

If the resistance of the coil is very small i.e., $\frac{1}{LC} \gg \left(\frac{R}{L}\right)^2$ then $\left(\frac{R}{L}\right)^2$ can be neglected.

$$\therefore \quad f_r = \frac{1}{2\pi\sqrt{LC}}$$

At this frequency the admittance is minimum (impedance is maximum) and hence current is minimum. This frequency is called resonant frequency.

Impedance at resonance:

The impedance at resonance is called ***'dynamic resistance'*** of the circuit. At resonance, the susceptive component of admittance is zero. Thus

$$\frac{1}{Z} = \frac{R}{R^2 + \omega_r L^2}$$, from eq. (1) but from eq.(2) $R^2 + \omega_r{}^2 L^2 = \frac{L}{C}$

$$\therefore \frac{1}{Z} = \frac{RC}{L}$$

or $$Z = \frac{L}{CR}$$

If the resistance 'R' is small the impedance is maximum. If 'R' is negligible, the impedance is infinite at resonance.

Frequency Response curve of parallel resonant circuit:

Frequency versus current curves are shown in fig (1).

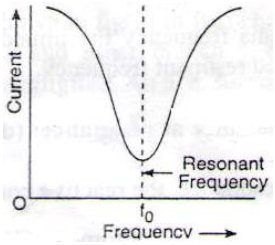


fig (1)

Band width:

In case of a parallel resonance circuit bandwidth is defined as the range of the frequencies where impedance falls to 70.7% of its maximum value at resonance as shown in fig. (1).

Q-factor of a parallel resonant circuit:

It is defined as ''ratio of the current circulating in its branches to the line current drawn from the supply or simply as current magnification''.

At resonance the current circulating between the capacitor or inductor is $i_c or i_L$ and current from the supply is i_r.

Hence, Q-factor = $\frac{i_c}{i_r} = \frac{i_L}{i_r}$

But $$i_c = \frac{V}{X_C} = \frac{V}{\frac{1}{\omega_r C}} = \omega_r CV$$

and $i_r = \frac{V}{L/CR} = \frac{CRV}{L}$ (since $\frac{L}{CR}$ is dynamic resistance at parallel resonance)

$$\therefore \quad Q = \frac{\omega_r CV}{CRV/L} = \frac{\omega_r L}{R} = \frac{2\pi f_r L}{R} \qquad \rightarrow (1)$$

At parallel resonant frequency, when R is small (negligible) $f_r = \frac{1}{2\pi\sqrt{LC}}$

Substituting the value of f_r in equation (1) we have $Q = \frac{2\pi L}{R}\frac{1}{2\pi\sqrt{LC}} = \frac{1}{R}\sqrt{\frac{L}{C}}$

Q. Compare series and parallel resonance in RLC circuits.

Series resonance	Parallel resonance
1.Impedance at resonance is minimum, Z=R	Impedance at resonance is maximum,Z=L/CR
2.Resonance frequency= $\frac{1}{2\pi\sqrt{LC}}$	Resonance frequency = $\frac{1}{2\pi}\sqrt{\frac{1}{LC} - \frac{R^2}{L^2}}$
3. Resonant frequency is independent of R.	Resonant frequency is dependent of R.
4. Current at resonance is Maximum.	Current at resonance is Minimum.
4. Power factor is Unity.	Power factor is Unity.
5. It is a Acceptor circuit.	It is a Rejecter circuit.
7. For high selectivity generator should have low internal impedance Z.	For high selectivity generator should have high internal impedance Z.
8. It is called as Voltage magnification circuit.	It is called as current magnification circuit.

BIPOLAR JUNCTION TRANSISTOR (BJT)

A **BJT** is a semiconductor three terminal device, invented in 1948 by Bardeen and Brattain of Bell labs, USA., which revolutionized the electronic industry and become the heart of most electronic instruments.

BJT's have now become the backbone of all modern communication and power systems and form the key elements in computers, space vehicles and satellites.

Types of Transistors, Structure and Circuit Symbols of Transistors:

A Bipolar Junction Transistor (BJT) or simply a Transistor is a sandwich of one type of semiconductor (p-type or n-type) between two types of the other type. Accordingly, there are two types of transistors:

(i) N-P-N transistor and (ii)P-N-P transistor.

Transistors are made either from Silicon (or) Germanium crystal. The structure and circuit symbol of NPN and PNP transistors are shown in fig (1).

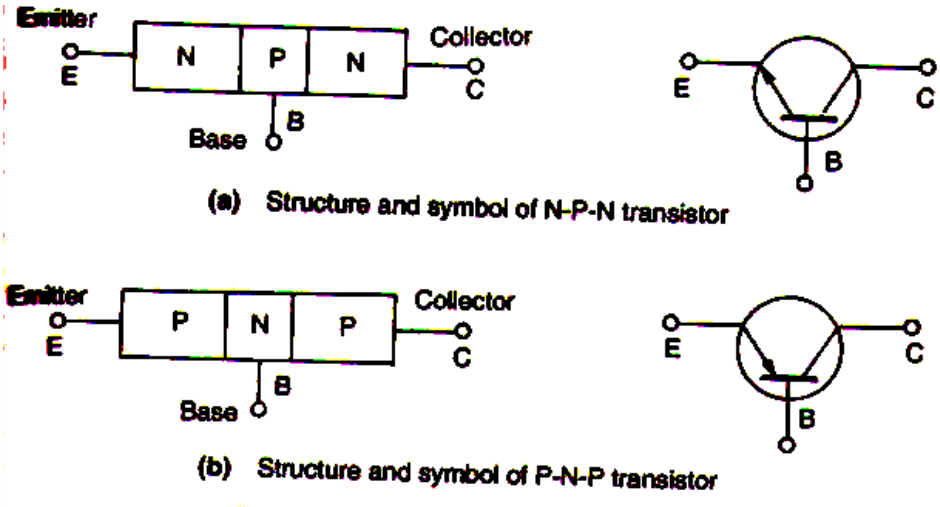


Fig.1(a) and (b) Structure & Circuit symbols of npn Transistor and pnp Transistor.

A transistor (NPN or PNP) have the following sections:

(i) Emitter: The main function of this region is to supply majority charge carriers (either electrons or holes) to the base and hence it is more heavily doped in comparison to base and collector.

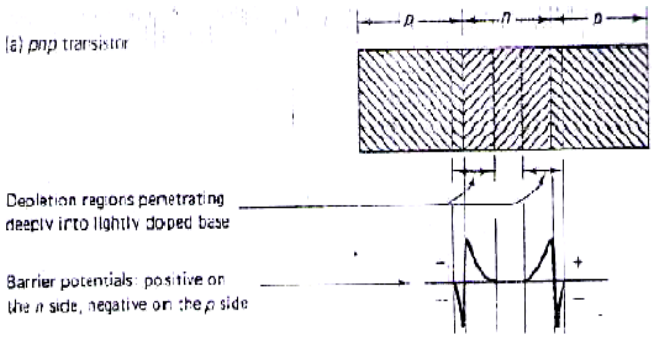
(ii) Base: The center region is called the Base. This is very lightly doped and is very thin (10^{-6}m) as compared to either emitter or collector so that it may pass most of the injected charge carriers to the collector.

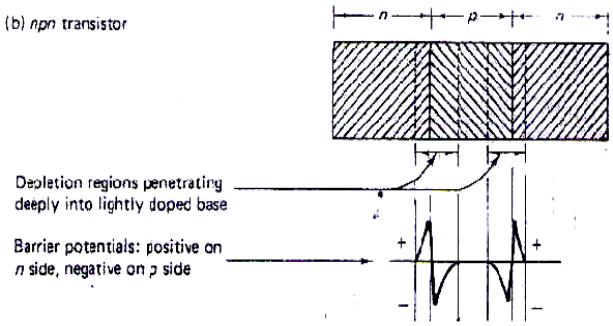
(iii) Collector: The main function of the collector is to collect majority charge carriers through the base. This is moderately doped.

In a circuit symbol, arrowhead is always at the emitter. It indicates the conventional current direction when EB junction is forward biased. In transistors, the collector region is made physically larger than the emitter region. This is due to the fact that collector has to dissipate much greater power. Due to this difference, the Collector and Emitter are not interchangeable.

Each transistor has two p-n junctions called the emitter –base (E-B)junction and collector –base (C-B) junction. The E-B junction is always forward biased while the C-B junction is reverse biased. Thus, the resistance of E-B junction is very small as compared to C-B junction.

Barrier potentials and depletion regions for unbiased transistors: Fig (2 a &2b), illustrate the depletion regions, barrier potentials and electric fields at the junctions of pnp and npn transistors .The outer layers i.e., E and C are much more heavily doped than the center layer B. this cause the depletion





region to penetrate

Fig.(2a) Fig.(2b)

deeply into the base and thus the distance between the EB and CB depletion regions is minimized.

Transistor Biasing: The transistor biasing is shown in fig (1). The E-B junction is always forward-biased while the C-B junction is always reverse biased for working of the transistor. For this purpose supply voltages V_{EE} is connected between E and B junction while V_{CC} is connected between C and B junction.

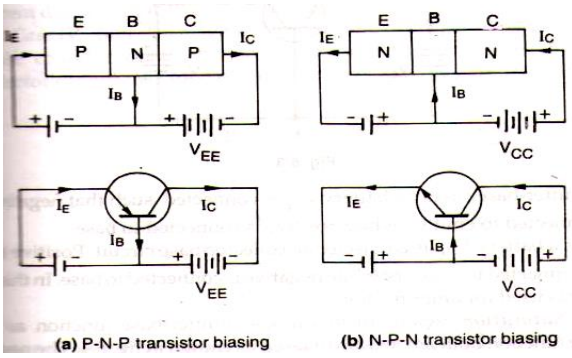
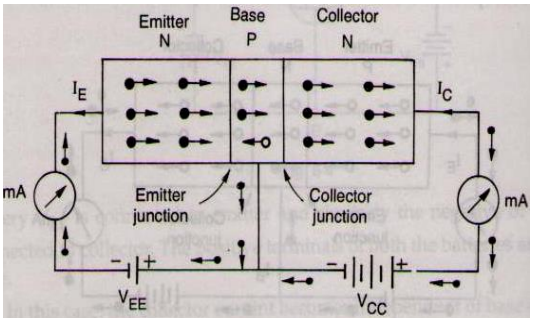


Fig.1. Transistor Biasing

The forward biasing of E-B junction allows a low resistance for emitter circuit and reverse-biasing of C-B junction provided high resistance in the collector circuit.

In transistor, a weak signal is introduced in low resistance circuit and output is taken from the high resistance circuit. So, a transistor transfers a signal from low resistive circuit to high resistive circuit. The prefix trans means the signal transfer property of the device while 'istor' classifies with resistors, so the name transistor is a contraction of words transfer and resistor.

Transistor working (working of NPN & PNP transistors): Fig(1) shows an NPN transistor with E-B junction as forward biased by the supply voltage V_{EE} and C-B junction as reverse biased by supply voltage, V_{CC}.



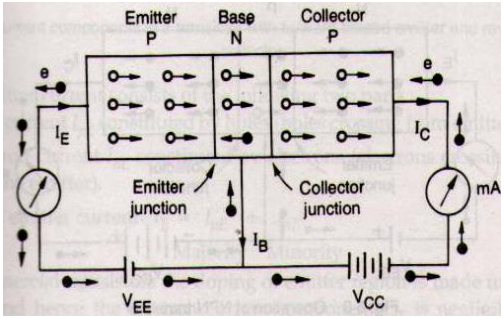


Fig.(1) Operation of npn Tr. Fig.(2) Operation of pnp Tr.

The forward bias at the E-B junction causes electrons to flow from the n-type emitter to the p-type base. The electrons are "emitted" into the base region, hence the name 'emitter'. Holes also flow from the p-type base to the n-type emitter, but since the base is much more lightly doped than the emitter, almost all of the current flow across the EB junction consists of electrons entering the base from the emitter. A very few electrons (2%) tends to recombine with holes in the p-type base region andconstitute base current I_B. The remaining (98%) electrons which appear as minority carriers in the p-type base and the reverse bias assist them to cross the junction. Hence, they are collected by collector. Now, the electrons in the n-region (collector) readily swept up by the positive collector voltage (V_{CC}) and constitutes collector current, I_C. So the current conduction in NPN transistor is carried by the electrons.

There is another small component of collector current due to thermally generated carriers due to reverse bias at CB junction. This current is called reverse saturation current I_{CBO} (I_{CO}). The conventional directions of emitter, base and collector currents are shown by I_E, I_B and I_C respectively.

Fig (2) shows a PNP transistor with E-B junction as forward biased and CB junction as reverse biased by V_{EE} and V_{CC} respectively. The forward bias at the EB junction reduces the potential barrier and hence the holes cross this junction and enter into N-type base region. This constitute the emitter current I_E. The width of the base region is very thin and it is lightly doped and hence only about 2% of the holes recombine with the free electrons of N-region (base) and constitute base current I_B. The remaining holes (98%) which appear as minority carriers in the n-type base and the reverse bias assists them to cross the junction (CB junction) and enter into to the collector. Hence, they are collected by the collector and forms collector current (I_C). Now, the holes in the p-region (collector) readily swept by the –ve collector voltage, V_{CC} and constitutes collector current I_C. So, the current conduction in PNP transistor is carried out by the holes.

There is another component of collector current due to thermally generated carriers due to reverse bias at CB junction. This current is called reverse saturation current, I_{CBO} (=I_{CO}). The conventional directions of emitter, base and collector currents are shown by I_E, I_B and I_C respectively.

Transistor Current and Voltage Notations:

Standard circuit notation is used for transistor circuit analysis.

For d c quantities: Emitter current I_E, collector current I_C , base current I_B, collector-emitter voltage V_{CE}, Emitter supply voltage V_{EE}, Base supply voltage V_{BB}, Collector supply voltage V_{CC}.

For a c quantities: $i_e, i_c, i_b, v_{ce}, v_{eb}, v_{cb}$

For rms values of ac currents: I_e, I_b, and I_c

The total ac and dc currents: Emitter current, i_E, collector current, i_C and base current, i_B

For example (i) $i_E = I_E + i_c$ (ii) $i_C = I_C + i_c$

(dc value) (ac value)

Currents components in a transistor

Fig (1) shows the various currents which flow across the forward biased EB junction and reverse biased CB junction in a PNP transistor. The emitter current consists two parts,

(i) hole current I_{PE} (holes crossing from E to B)

(ii) Electron current I_{nE} (electrons crossing from B to E).

Therefore total emitter current, $I_E = I_{pE} + I_{nE}$

(Majority) (Minority)

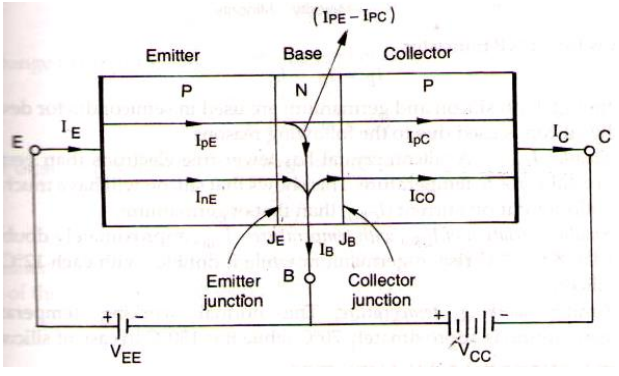


Fig.(1) current components in Tr

Since the emitter region is made much heavily doped than base, I_{nE} is negligible. Thus in a PNP transistor the emitter current I_E (= I_{pE}) consists almost entirely of holes. A few of holes crossing the EB junction recombine with the electrons in n-type base and rest of them cross the CB junction.

If I_{pC} is the hole current at CB junction, the difference (I_{pE} - I_{pC}) is the recombination current I_B which leaves the base as shown in fig (1). The holes on reaching the CB junction cross this junction and enter the p-region (collector).

If the emitter is open-circuited, then I_E=0, i.e., I_{pC} would be zero. Under this condition, at the reverse biased CB junction, due to minority carriers flow, there is a collector current I_C equals the reverse saturation current I_{CBO}, which consists of two parts

(i) I_{nco} caused by electrons crossing from C to B and (ii) I_{pco} caused by holes crossing from B to C

$$\therefore \quad I_{CBO} = I_{nco} + I_{pco}$$

$$\text{In general} \quad I_C = I_{pC} + I_{CBO}$$

(Majority) (Minority)

Fig (1) shows that I_E flows into the transistor for a PNP transistor and that both I_B and I_C flow out of the transistor. $\therefore \quad \mathbf{I_E = I_C + I_B}$

Transistor circuit configurations: A transistor may be connected by connecting one of the three terminals E,B and C to the ground.. Accordingly, there are three types of transistor circuit configurations. They are (i) Common –base (CB) (ii) Common –emitter (CE) (iii) common-collector (CC).

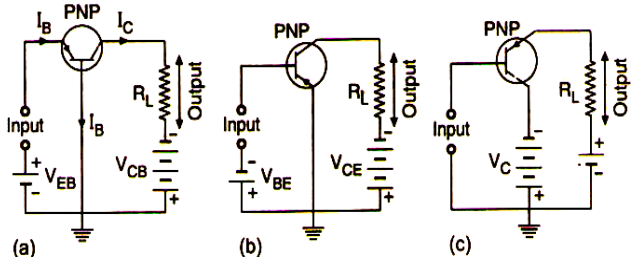


Fig.(1) different configurations of PNP Tr.

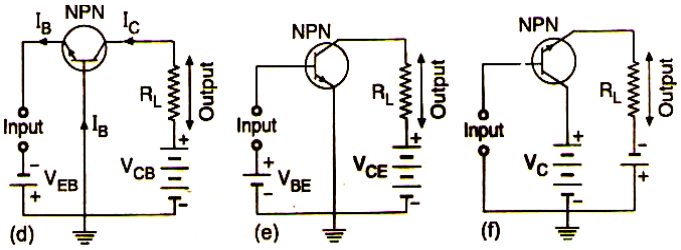


Fig. (2) different configurations of NPN Tr.

Regardless the circuit configuration the EB junction is always forward biased and CB junction is always reverse biased. The different configurations of PNP and NPN transistors are shown in Fig (1. (a), (b), (c) and fig.(2) (d) (e) (f) respectively.

Constants of a Transistor:

In a common base circuit, the collector current I_C is controlled by the variations of emitter current I_E i.e., if I_E is changed by changing forward bias voltage at E-B junction, the I_C will also change.

Current amplification factor in common base configuration (α) "The ratio of change in collector current (ΔI_C) to the change in emitter current (ΔI_E) when collector to base voltage V_{CB} is maintained at a constant value, is called the current amplification factor,**(α).**"

$$\text{Mathematically} \qquad \alpha = \frac{\Delta I_C}{\Delta I_E} \Big|_{V_{CB} = \text{constant.}} \rightarrow \qquad (1)$$

In CB configuration, since I_C is slightly less than I_E, α is always slightly less than unity. Its value lies between 0.95 to 0.995.

In a common emitter circuit, the input signal is applied to the base and emitter and the output is taken from collector to emitter.

Current amplification factor in common emitter configuration (β):

"The ratio of change in collector current (ΔI_C) to the change in base current (ΔI_B) when the collector to emitter voltage (V_{CE}) is maintained at a constant value is known as the current amplification (β)".

Mathematically,

$$\beta = = \frac{\Delta I_C}{\Delta I_B} \mid V_{CE} = \text{constant} \rightarrow \quad (2)$$

Since small changes in I_B produces large changes in I_C, the value of β is always greater than unity, usually, β ranges from 20 to 500.

Relation between α & β:

Since α and β are characteristics of a particular transistor, they must be related to each other.

For a transistor, $I_E = I_C + I_B$

For small changes in currents, we have

$$\delta I_E = \delta I_B + \delta I_C$$

Dividing throughout by δI_C, we get $\frac{\delta I_E}{\delta I_C} = \frac{\delta I_B}{\delta I_C} + \frac{\delta I_C}{\delta I_C} = \frac{\delta I_B}{\delta I_C} + 1$

Substituting $\frac{\delta I_E}{\delta I_C} = \frac{1}{\alpha}$ and $\frac{\delta I_B}{\delta I_C} = \frac{1}{\beta}$

We get $\frac{1}{\alpha} = \frac{1}{\beta} + 1 = \frac{1+\beta}{\beta} \quad \therefore \quad \alpha = \frac{\beta}{1+\beta} \quad \rightarrow (1)$ (α in terms of β)

β in terms of α: we have $\alpha = \frac{\beta}{1+\beta}$

Or $\alpha(\beta+1) = \beta \Rightarrow \alpha + \alpha\beta = \beta$

$\Rightarrow \alpha = \beta - \alpha\beta$ or $\alpha = \beta(1-\alpha)$

$$\beta = \frac{\alpha}{1-\alpha} \rightarrow (2)$$

It is obvious that, as α approaches towards unity, β goes on increasing.

If α =0.98, β =49, but if α =0.99, then β = 99.

Problem: The current gain of a transistor in CE circuit is 49. Calculate its CB current gain. Find the I_B where I_E =3mA.

Solution: It is given that $\beta = 49$, and I_E =3mA.

We have, $\alpha = \frac{\beta}{1+\beta} = = \frac{49}{50} = 0.98$

We have, $I_C = \alpha I_E = 0.98 \times 3 = 2.94\text{mA}$

$\therefore I_B = I_E - I_C = 3 - 2.94 = 0.06\text{mA}$

$\therefore I_B = 0.06\text{mA} = 60\,\mu A$

Transistor Leakage currents:

Collector to Base leakage current I_{CBO}: In common base configuration, if emitter circuit is open [Fig (1)], even then a small current flows in collector base circuit.

This current is due to the motion of minority carriers across collector base junction on due to its reverse bias. It is known as collector to base leakage current with emitter open, I_{CBO}. This is shown in fig (1).

Expression for Collector current:

(1) Collector to Base leakage current: In common base configuration, if emitter circuit is open fig(1),even then a small current flows in collector base circuit. This is due to the motion of minority carriers across collector base junction on account of it being reverse biased. It is known as collector to base leakage current with emitter open, I_{CBO}. This is shown in fig (1).

Expression for collector current

In common base arrangement of transistor, the collector current is made two parts:

(i) αI_E i.e., part of I_E which reaches the collector and

(ii) I_{CBO} i.e., collector to base leakage current.

Therefore, collector current, $I_C = \alpha I_E + I_{CBO} \rightarrow (1)$

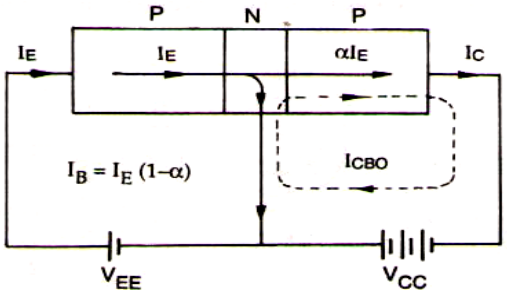


Fig.(1) showing leakage current, I_{CBO}

The collector current can also be expressed as $I_C = \alpha I_E + I_{CBO}$

or $I_C = \alpha(I_C + I_B) + I_{CBO} \quad (\because I_E = I_B + I_C)$

or $I_C(1-\alpha) = \alpha I_B + I_{CBO}$

or $I_c = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CBO} \rightarrow (2)$

$\therefore I_C = \beta I_B + (1+\beta) I_{CBO} \rightarrow (3) \quad [\because \beta = \frac{\alpha}{1-\alpha} \; and \; (1-\alpha) = \frac{1}{1+\beta}]$

(2). Collector to Emitter leakage current, I_{CEO}.: In common emitter configuration, if base circuit is open [fig (2)], even then a small current flows in collector to emitter circuit. It is known as collector to emitter leakage current with base open, I_{CEO}. This is shown in fig (2).

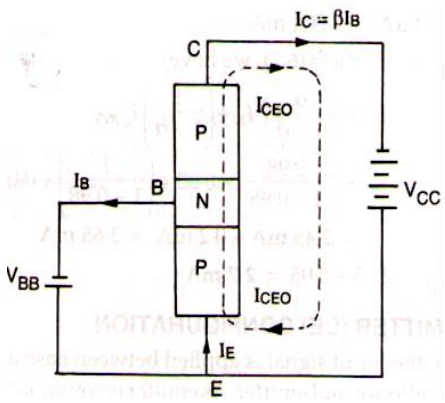


Fig.(2) showing leakage current

Expression for collector current: In common emitter arrangement of transistor, the collector current I_C is given by [from (2)], $I_C = \beta I_B + I_{CEO} \rightarrow (4)$

We have, $I_c = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CBO} \rightarrow (5)$ [from (2)]

Comparing the equations (4) and (5), we get

$$\beta = \frac{\alpha}{1-\alpha} \quad \text{and} \quad I_{CEO} = \frac{1}{1-\alpha} I_{CBO} = (\beta + 1) I_{CBO}$$

(3). In common collector configuration, I_E is the output current and I_B is the input circuit current. The current amplification factor in CC configuration is given by 'γ' (gama)

$$\gamma = \frac{I_E}{I_B}, \text{ we have } I_E = I_B + I_C \Rightarrow I_B = I_E - I_C$$

$$\text{Now } \gamma = \frac{I_E}{I_B - I_C} = \frac{I_E/I_E}{I_E/I_E - I_C/I_E} = \frac{1}{1-\alpha} \quad (\because \alpha = \frac{I_C}{I_E})$$

$$\therefore \gamma = \frac{1}{1-\alpha}, \text{ but } (1-\alpha) = \frac{1}{(1+\beta)}$$

$$\therefore \gamma = \frac{1}{1-\alpha} = (\beta + 1)$$

Comparison of different characteristics of transistor configurations:

S.No.	Characteristic	Common base	Common emitter	Common collector
1.	I/P resistance	Low about (100Ω)	Low	Very high
2.	O/P resistance	Very high about 400KΩ	High about 50 KΩ	Low about 50Ω
3.	Voltage gain	About 150	About 500	Less than 1
4.	Applications	At high frequencies	At, A.F.frequencies	Impedance matching

Transistor as an amplifier:

Fig (1) shows the basic circuit of transistor amplifier. The DC supply voltages V_{EE} and V_{CC} provide proper biasing to the transistor.In the circuit, the small signal to be amplified is applied between E-B circuit and output is taken across the load resistor R_L.

A small change in signal voltage produces an appreciable change in the emitter current, because the i/p circuit has low resistance due to FB. Now, due to transistor action, the change in I_E causes almost the same change in I_C. When that I_C flows through the load R_L, a large voltage is developed across it. Therefore, transistor acts as an amplifier.

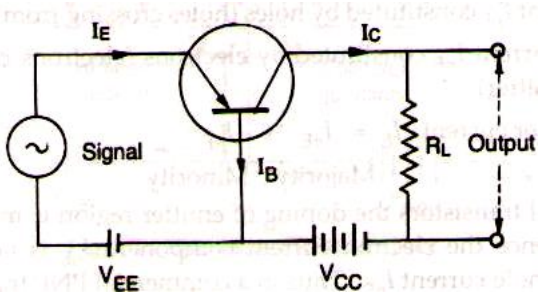


Fig.(1) Transistor as an amplifier

Let a small voltage change ΔV_i between E&B cause a relatively large emitter current change (ΔI_E) and hence large collector current change (ΔI_i), which is collected and passes through R_L. Thus

$$\alpha = \frac{\Delta I_C}{\Delta I_E};\ \text{i.e.,}\quad \Delta I_C = \alpha \Delta I_E \ \longrightarrow\ (1)$$

The change in o/p voltage across the load R_L, $\Delta V_o = R_L.\Delta I_c = R_L.\alpha\Delta I_E$ ($\because$ from 1)

$\therefore$ The voltage amplification A $= \frac{\Delta V_O}{\Delta V_i}$, will be greater than unity and the transistor acts as an amplifier.

Problem: A CB transistor amplifier has an input resistance of 20Ω and output resistance of 100KΩ. If a signal of 400 mV is applied between emitter and base, find voltage amplification. Assume $\alpha = 1$.

Solution:

The emitter current is given by, I_E = signal voltage/ input resistance = $\frac{400mV}{20\Omega}$ = 20 mA

Therefore, $I_C = \alpha I_E$ =1 × 20 mA = 20mA.

Now, output voltage, $V_O = I_C R_L$ = 20mA × 100K Ω =2000V

$\therefore$ Voltage amplification, A $= \frac{V_O}{V_i} = \frac{2000V}{400mV} = 5000$

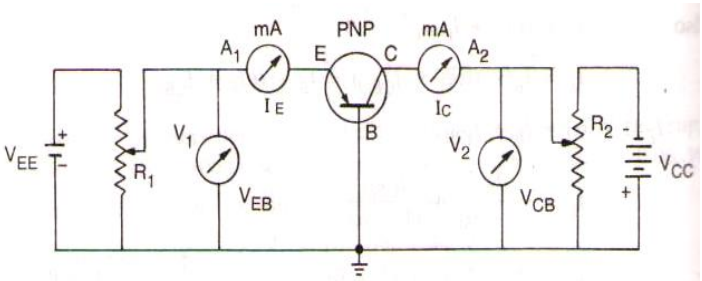
Transistor Characteristics Curves:

Transistor characteristics are the curves that relate transistor currents and voltages. They help to find transistor's parameters.

Transistor characteristics curves can be drawn in any one of the three configurations, common base, common emitter and common collector.

Characteristics of common-base (CB) configuration:

Fig (1) shows the experimental arrangement to draw the input and output characteristics of pnp transistor in CB configuration.



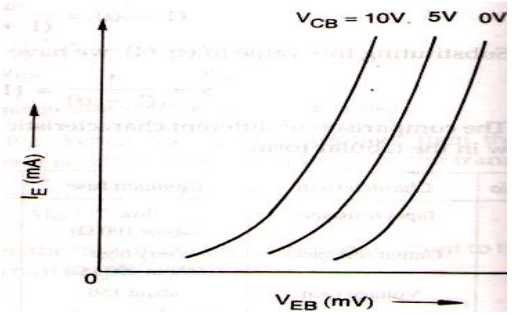


Fig.(1) PNP transistor connected in CB configuration **Fig.(2) Input characteristics**

The supply voltage V_{EE} and V_{CC} provide forward and reverse bias voltages at EB junction and CB junction respectively. The voltage V_{EE} and hence I_E can be varied with the help of potentiometer R_1 and the voltage V_{CB} and hence I_C can be varied with the help of potentiometer R_2. The d c milli-ammeters and voltmeters connected in the circuit measure the dc currents and voltages. The graphical relationships between the dc voltages and currents drawn give the input and output characteristic curves of a transistor.

Input characteristics: "The curve between I_E and V_{EB} at a constant voltage V_{CB} represents the input characteristic of a transistor."

To plot the input characteristic, the voltage V_{CB} is kept fixed. The voltage V_{EB} is varied in steps and the current I_E is noted for each value of V_{EB}. A graph of I_E against V_{EB} is drawn. The curve is known as input characteristic. The experiment is repeated for the other fixed values of V_{CB}. The input characteristics are shown in fig (2). The following points are noted from the characteristics.

(i) There exists a cut in or offset or threshold voltage V_{EB} below which the emitter current, I_E is very small.

(ii) The emitter current, I_E increases rapidly with small increase in emitter-base voltage V_{EB}. It means that input resistance is very small.

Output characteristics: "The curve drawn between I_C and V_{CB} at a constant emitter current I_E represents the output characteristics of a transistor."

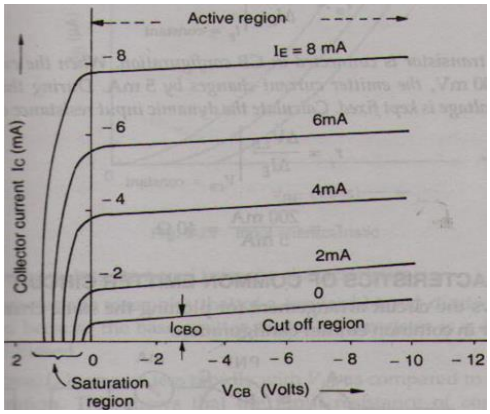


Fig.(3) Output characteristics

To plot the output characteristics, the emitter current I_E is kept fixed. With the help of the potentiometer R_2, the value of V_{CB}, is varied insteps and collector current I_C noted for each value of V_{CB}. The curve so obtained is known as output characteristic. The experiment is repeated for fixed values emitter current I_E. Fig (3) shows the output characteristics. The following points are noted from the characteristics.

(i) In the "active region", the collector current, I_C is essentially independent of collector voltage, V_{CB} and depends only upon emitter current I_E.

(ii) Although I_C is practically independent of V_{CB}, if V_{CB} is increased further the collector current increases rapidly due to avalanche Break down. [This is not shown in fig (3)]

(iii) In the "cut-off region," a small amount of collector current I_C flows even when emitter current I_E =0. This is the collector leakage current I_{CBO}.

(iv) In the "saturation region", the collector current I_C flows even when V_{CB} =0. Here, both EB junction and CB junction are forward biased.

(v) A very large change in the collector to base voltage, V_{CB} produces only a small change in the Collector current I_C. It means that the output resistance is very high.

(vi) The collector current I_C is always a little less than the corresponding emitter current, I_E (due to a small percentage of charge carriers being lost in the base due to electron-hole combination.)

Characteristics of common emitter configuration:

Fig (1) shows the experiment arrangement to draw the input and output characteristics of PNP transistor in CE configuration. The supply voltage V_{BB} provides forward bias at EB junction and V_{CC} provides reverse bias at CB junction. The voltage V_{BE} and hence current I_B can be varied with the help of potentiometer R_1 and the V_{CE} and I_C can be varied with the help of R_2. The dc micro and milli-ammeter and voltmeter connected in circuit to measure dc currents and voltages. The graphical relationship between the dc voltages and currents drawn gives the input and output characteristic curves of a transistor.

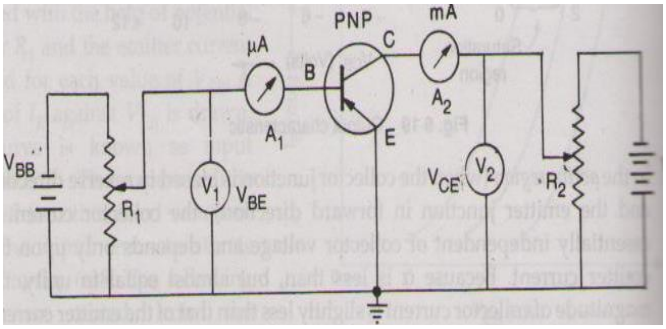


Fig.(1) PNP transistor connected in CE mode

Input characteristics:

The curve drawn between base current I_B and base-emitter voltage V_{BE} at a constant collector - emitter voltage V_{CE} represents the input characteristic curve of a transistor.

To plot the input characteristic curve, the voltage V_{CE} is fixed. The voltage V_{BE} is varied with the help of potentiometer R_1 and the base current I_B is noted for each value of V_{BE}. A graph of I_B against V_{BE} is drawn. The curve so obtained is known as input characteristic. The experiment is repeated for other values of V_{CE}. The input characteristic curves are shown in Fig (2). The following points are noted from the characteristic curves.

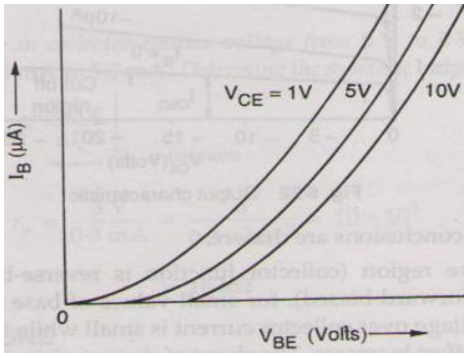


Fig.(2) input characteristics

(i) The input characteristic curves resemble to those of a forward biased junction diode.

(ii) The base current I_B increases non-linearly with increase in base voltage V_{BE}.

(iii) The base current I_B increases less rapidly with V_{BE} as compared in common base configuration.

(iv) Input characteristic curves are only dependent upon the V_{CE}.

Output characteristics:

The curve drawn between collector current I_C and voltage V_{CE} at constant base current I_B represents the output characteristic curve of a transistor.

To plot the output characteristics, the base current I_B is kept fixed. With the help of the potentiometer R_2, the value of V_{CE} is varied in steps and I_C is noted for each value of V_{CE}. A graph of I_C against V_{CE} is drawn. The curve so obtained is known as output characteristic. The experiment is repeated for different values of I_B. Fig (3) shows the output characteristics.

The following points are noted from the characteristics.

(i) In the "active region" for small values of I_B, the effect collector to emitter voltage, V_{CE} over collector current I_C is small, while for large values of t I_B this effect increase. Here, the collector current I_C is larger than input current I_B. Thus, there is a current amplification. The operation of the transistor, when used as an amplifier must be restricted in the "active region" only.

(ii) In the" saturation region" i.e., when V_{CE} is very low, the change in I_B does not produce a corresponding change in I_C.

(iii) When V_{CE} is allowed to increase too high, the CB junction breaks down due to avalanche breakdown and then I_C increases rapidly and hence the transistor is damaged.

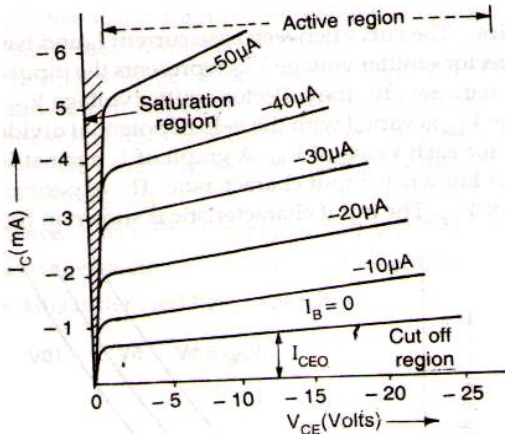


Fig.(3) output characteristics

(vi) In the "cutoff region" a small amount of I_C flows even when $I_B = 0$. This is called leakage current I_{CEO}. Since $I_C = 0$, the transistor is said to be cutoff.

Problems 1: A transistor has I_{CBO}=48nA and $\alpha = 0.992$, find β, I_{CEO} and I_C when $I_B = 30\,\mu A$.

Solution: Given $I_{CBO} = 48\text{mA} = 48\times10^{-9}$ A, $\alpha = 0.992$

(i) $\beta = \alpha/1-\alpha$ = 0.992/1 - 0.992 = 0.92/0.008 = 124

(iii) $I_{CEO} = (1+\beta)I_{CBO} = (1+124).48\times10^{-9}\text{A} = 6000\times10^{-9}\text{A} = 6\,\mu A$

(iii) Given, $I_B = 30\,\mu$ A $\therefore I_C = \beta I_B + (1+\beta) I_{CBO}$ = 124(30X10^{-6})+ (1+124) 48X10^{-9}

= 3.72X10^{-3}+6000X10^{-9}A = 3726X10^{-6}A = 3.726mA

The two port network & h-parameters

Consider a two port network or four terminal network contained in block box as shown in fig (1). As matter of convention, currents flowing into box are taken as +ve and similarly voltages are +ve from upper to the lower terminals .In fig (1), port $1(1,1')$ is connected to energy source and port $(2,2')$ connected to the load. Port 1 is called input port and port 2 is known as output port.

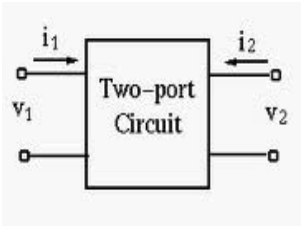


Fig.(1)

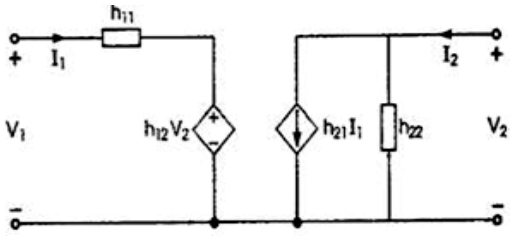


Fig.(2) Hybrid parameter equivalent ckt.

The behavior of a two port network now may be expressed in terms of the four quantities, the input and output currents (i_1, i_2) and the voltages (v_1, v_2) at the ports. Among the four variable quantities any two may be chosen as independent variables (i_1, v_2) leading two equations which may be solved for the two dependent variables (v_1, i_2). Then the two equations are

$$v_1 = h_{11}i_1 + h_{12}v_2 \rightarrow (1)$$

$$i_2 = h_{21}i_1 + h_{22}v_2 \rightarrow (2)$$

If output port is short circuited, then $v_2 = 0$ and equation (1) gives,

$h_{11} = \frac{v_1}{i_1} = h_i$, the input impedance ($\Omega$) with output port is short circuited.

$h_{21} = \frac{i_2}{i_1} = h_{f,}$ Forward transfer current gain with output port short circuited.

If the input port is open circuited then $i_1 = 0$ and equation (2) gives,

$h_{12} = \frac{v_1}{v_2} = h_r$, Reverse voltage gain with input port open circuited.

$h_{22} = \frac{i_2}{v_2} = h_o$, The output admittance with input open circuited

Since $h_{11}, h_{21}, h_{12}, \& h_{22}$ are different parameters having different units and hence they are called hybrid or h-parameters.

The h-parameters equivalent circuit of the two ports network, as derived from equations (1) & (2) is shown in fig (2).

CE configuration as a two port network & h-parameters.

The two port representation of a transistor in CE mode is shown in fig (1). To amplify low frequency a c voltage of small amplitude (called signal) is applied to the input port and the amplified signal is taken at the output port of the transistor amplifier.

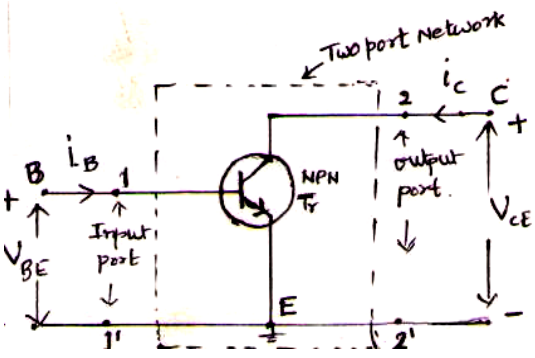


Fig.(1) Two port representation of CE Amp

The signal currents are i_B and i_C and the voltages are v_{BE} and v_{CE}. For a transistor in CE mode the current i_B and voltage v_{CE} are independent variables and the voltage v_{BE} and current i_C are dependent variables. Then the equations are

$$v_{BE} = h_{ie} i_B + h_{re} v_{CE} \rightarrow (1)$$
$$i_C = h_{fe} i_B + h_{oe} v_{CE} \rightarrow (2)$$

Here, $h_{ie,} h_{fe,} h_{re}$ and h_{oe} are of different parameters of a transistor and they are termed as h-parameters or hybrid parameters.

Definitions of h-parameters if CE configuration

$h_{ie} = \frac{v_{BE}}{i_E} \mid v_{CE} = 0$, is the input impedance when output is short circuited to ac. Its unit is ohms.(Ω)

$h_{re} = \frac{v_{BE}}{v_{CE}} \mid i_B = 0$, is the reverse voltage gain when the input is open circuited to ac.

$h_{fe} = \frac{i_C}{i_B} \mid v_{CE} = 0$, is the forward current gain when the output port is short circuited.

$h_{oe} = \frac{i_C}{v_{CE}} \mid i_B = 0$, is the output admittance when the input port is open circuited to ac. its unit is mhos. (Simen)

As $h_{ie,} h_{fe,} h_{re}$ and h_{oe} are of different parameters having different units, they are termed as the h-parameters of CE amplifiers.

The hybrid equivalent circuit of CE amplifier.

Consider the CE npn transistor circuit shown in fig(1a), where R_g is the generator resistance of the input signal and R_L is the load resistance. The equations of fig (1a) are

$v_i = v_{BE} = h_{ie} i_B + h_{re} v_{CE} \rightarrow (1)$ and $i_C = h_{fe} i_B + h_{oe} v_{CE} \rightarrow (2)$, where $v_o = v_o = v_{CE}$

From equation (1), we get

$i_B = \frac{v_{BE} - h_{re} v_{CE}}{h_{ie}}$ or $i_B = \frac{v_i - h_{re} v_o}{h_{ie}} \rightarrow (3)$ and

From equation (2), we get $h_{fe} i_B = -h_{oe} v_{CE} + i_C \rightarrow (2)$. Fig.(1b) shows the hybrid equivalent circuit of CE amplifier shown in Fig.(1a).

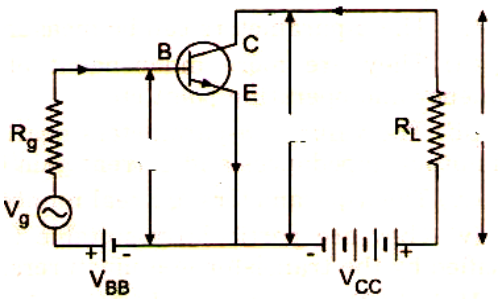


Fig.(1a)

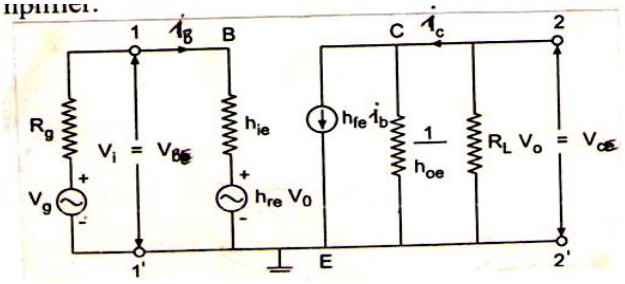


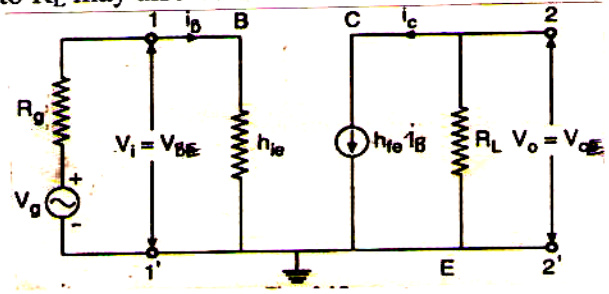
Fig.(1b)

Simplified hybrid equivalent circuit of CE amplifier.

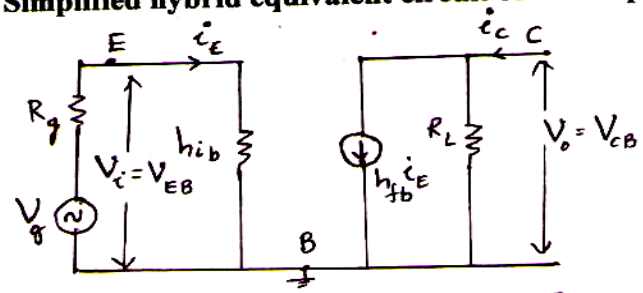
In transistor h_{re} is very small (=10^{-4}) and hence $h_{re}\, v_O$ may be omitted in simplified equivalent circuit. Also, h_{oe} of a transistor is $\approx 10^{-5}$ mhos, so $\frac{1}{h_{oe}}$ is $\approx 10^5\ \Omega$ and hence $\frac{1}{h_{oe}} > R_L$

Therefore, $\frac{1}{h_{oe}}$ which is parallel to R_L may also be omitted from the simplified hybrid equivalent circuit, and is shown in fig (1).

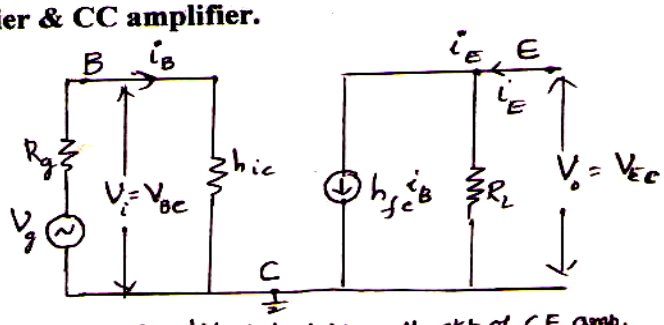
Fig(1)



Simplified hybrid equivalent circuit of CB amplifier & CC amplifier.



Fig(2) Simplified hybrid equt. ckt of CB ampr.



Fig(3). Simplified hybrid equelt ckt of CE amp.

Analysis of a CE transistor Amplifier using h-parameters:

The low frequency hybrid parameters (h-parameters) equivalent circuit of CE transistor amplifier circuit drawn in fig (1) is shown in fig (2). Now with the help of h-parameters equivalent circuit we will derive expressions for current gain, input impedance voltage gain, output impedance and power gain.

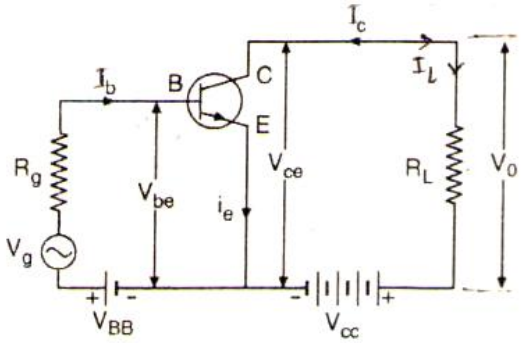


Fig (1)

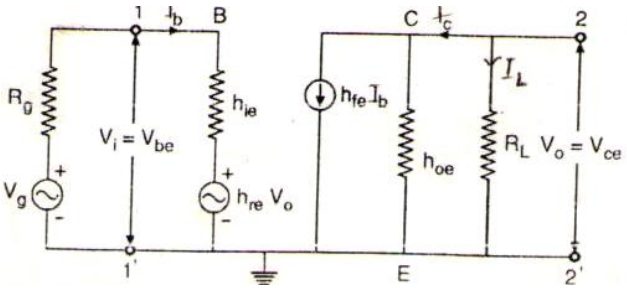


Fig (2)

The h-parameters equations for fig (1) are given by,

$$V_{be} = h_{ie}I_b + h_{re}V_{ce} \quad \rightarrow(1)$$
$$I_c = h_{fe}I_b + h_{oe}V_{ce} \quad \rightarrow(2)$$
$$\text{and } V_{ce} = -I_cR_L \quad \rightarrow(3)$$

Current gain (A_{ie}): It is defined as "the ratio of the output current to the input current". If I_L is the load current through the load resistanceR_L, then

$$A_{ie} = \frac{I_L}{I_b} = -\frac{I_c}{I_b} \quad \rightarrow(4)$$

Substituting the value of V_{ce} from equation (3) in equation (2), we get

$$I_c = h_{fe}I_b + h_{oe}(-I_cR_L)$$
$$\text{Or } I_c = h_{fe}I_b - I_ch_{oe}R_L$$
$$\text{Or } I_c + I_ch_{oe}R_L = h_{fe}I_b$$
$$\text{Or } I_c(1 + h_{oe}R_L) = h_{fe}I_b$$
$$\text{Or } \frac{I_c}{I_b} = -\frac{h_{fe}}{1+h_{oe}R_L} \quad \rightarrow(5)$$

Substituting this value in equation (4), $A_{ie} = -\frac{I_c}{I_b} = -\frac{h_{fe}}{1+h_{oe}R_L}$

$$\therefore A_{ie} = -\frac{h_{fe}}{1+h_{oe}R_L}$$

Input impedance: This is defined as "the ratio of the input voltage across the input terminals of the amplifier, i.e V_{be} to the current, I_b."

$$\therefore Z_{ie} = \frac{V_{be}}{I_b} \quad \rightarrow(6)$$

But $V_{be} = h_{ie}I_b + h_{re}V_{ce} = h_{ie}I_b + h_{re}(-I_cR_L) \quad (\because V_{cc} = -I_cR_L)$

$$\therefore Z_{ie} = \frac{V_{be}}{I_b} = h_{ie} - h_{re}R_L\left(\frac{I_c}{I_b}\right) = h_{ie} + h_{re}R_LA_{ie}$$
$$Z_{ie} = h_{ie} + h_{re}R_L\left(-\frac{h_{fe}}{1+h_{oe}R_L}\right) \quad \left(\because A_{ie} = -\frac{h_{fe}}{1+h_{oe}R_L}\right)$$
$$\therefore Z_{ie} = h_{ie} - \frac{h_{fe}h_{re}R_L}{1+h_{oe}R_L}$$

Voltage gain: It is defined as "the ratio of the output voltage to the input voltage", denoted by A_{ve}

$$\text{i.e., } A_{ve} = \frac{V_{ce}}{V_{be}} = \frac{-I_cR_L}{V_{be}} = -\frac{I_c}{I_b}.\frac{I_b}{Vbe}R_L = A_{ie}\frac{1}{Z_{ie}}R_L$$
$$A_{ve} = A_{ie}\frac{1}{Z_{ie}}R_L \quad \rightarrow(7)$$

Substituting the value of A_{ie} and Z_{ie} in equation (7), we have

$$A_{ve} = \left(-\frac{h_{fe}}{1+h_{oe}R_L}\right)\left(\frac{1}{h_{ie}-\frac{h_{fe}h_{re}R_L}{1+h_{oe}R_L}}\right)R_L$$

$$A_{ve} = -\frac{h_{fe}}{(1+h_{oe}R_L)}\frac{(1+h_{oe}R_L)}{[h_{ie}(1+h_{oe}R_L)-h_{fe}h_{re}R_L]}R_L$$

$$A_{ve} = \frac{-h_{fe}R_L}{h_{ie}+R_L[h_{ie}h_{oe}-h_{fe}h_{re}]}$$

Output impedance (Z_{oe}): The output impedance of the amplifier is obtained by setting V_{be} to zero, (fig (3)), R_L Infinity and driving the output terminals from a generator of voltage $V_o = V_{ce}$. If the current drawn from the source is I_c, the output impedance, i.e., $Z_{oe} = \frac{V_{ce}}{I_c}$

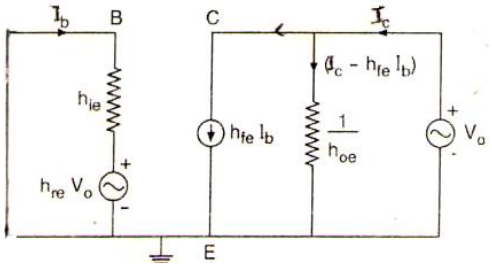


Fig (3) to find Z_{oe}

From equation (2), we have

$$I_c = h_{fe}I_b + h_{oe}V_{ce} \quad \rightarrow(8)$$

or $$\frac{I_c}{V_{ce}} = h_{fe}\frac{I_b}{V_{ce}} + h_{oe} \quad \rightarrow(9)$$

From equation (1), we have

$$0 = h_{ie}I_b + h_{re}V_{ce} \quad (\because V_{be} = 0, R_L = \infty)$$

or $$\frac{I_b}{V_{ce}} = \frac{-h_{re}}{h_{ie}} \quad \rightarrow(10)$$

From equations (9) and (10) we get

$$\frac{I_c}{V_{ce}} = h_{fe}\left(-\frac{h_{re}}{h_{ie}}\right) + h_{oe} = \frac{(h_{oe}h_{ie}-h_{fe}h_{re})}{h_{ie}}$$

$$Z_{oe} = \frac{V_{ce}}{I_c}$$

$$\therefore \quad Z_{oe} = \frac{h_{ie}}{(h_{oe}h_{ie}-h_{re}h_{fe})}$$

Power gain: It is simply defined as the product of the current gain and voltage gain. Thus A_{pe} is given by

$$A_{pe} = A_{ve} \times A_{ie}$$

Substituting the values of, A_{ve} and A_{ie},

$$A_{pe} = \left(\frac{-h_{fe}R_L}{h_{ie}+R_L(h_{ie}h_{oe}-h_{fe}h_{re})}\right) \times \left(-\frac{h_{fe}}{1+h_{oe}R_L}\right)$$

$$A_{pe} = \frac{{h_{fe}}^2 R_L}{(h_{ie}+R_L(h_{ie}h_{oe}-h_{re}h_{fe}))(1+h_{oe}R_L)}$$

Transistor Biasing & Load line analysis:

Transistor Biasing & Load line analysis:

- Biasing means to apply appropriate dc voltages and currents to a transistor in amplifier circuits.
- For proper operation of transistor the E/B junction must be forward biased and the C/B junction reverse biased.
- The dc load line is a line drawn on the output characteristics of a CE transistor joining the cutoff and saturation points.
- The intersection of dc load line, with the output characteristics of calculated I_B is known as Q-point.
- The Q-point specifies the dc output voltage and current when there is no ac input signal.
- By proper biasing of a transistor, a desired Q-point is obtained. This desired Q-point must be stable irrespective of changes in temperature or transistor parameters.
- The operating point (Q-point) of a transistor amplifier shifts with changes in
  - i. temperature variations and
  - ii. replacement of transistor by another of the same type due to inherent variations in transistor parameters β, V_{BE} and I_{CO}.
- The process of making Q-point independent of temperature changes or changes in transistor parameters is known as 'stabilization'.
- **DC-load line & Determination of Q-point:**

A dc load line is a straight line drawn on the output characteristics of a CE amplifier, to determine operating (Q-Point) point current and voltages in amplifier circuit, when no input signal is applied.

Consider a common emitter NPN transistor circuit of fig (1), when no input signal is applied.

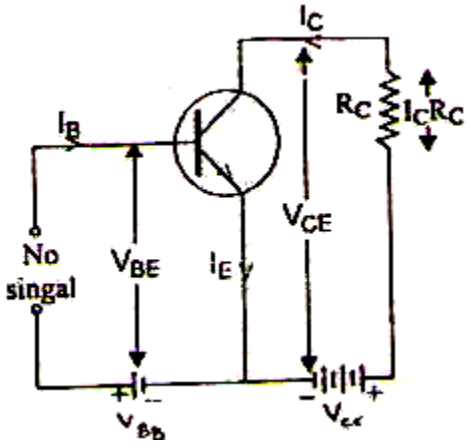


Fig.(1)

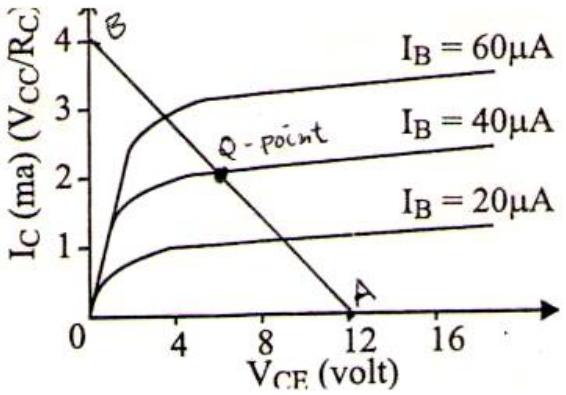


Fig.(2)

Applying KVL to the output loop of fig (1), $V_{CC} - I_C R_C - V_{CE} = 0$

$$\Longrightarrow \quad V_{CE} = V_{CC} - I_C R_C \rightarrow (1)$$

This equation gives $I_C = \left(-\frac{1}{R_C}\right) V_{CE} + \frac{V_{cc}}{R_c} \rightarrow (2)$

Equation (2) represents an equation of a straight line y= m x+ c → (3).

Therefore, if I_C is plotted against V_{CE} (on the output characteristics of CE transistor), we get a straight line, as shown in fig (2). This line is called the **dc load line**, with a slope m= $(-1/R_C)$. The two points of the line are located as follows.

(i) When $I_C = 0$, then $V_{CE} = V_{CC}$ from equation (1).

Thus we get point A, known as cutoff point.

(ii) When V_{CE} =0, then $I_C = V_{CC}/R_C$ from equation (2).

Thus we get point B, known as saturation point.

The line joining these two points A and B, on the output characteristics of CE transistor is called dc load line.

Determination of Q-point:

The operating point (Q-point) can be determined graphically, if I_B is known. I_B can be calculated using the relation $I_B = (V_{BB} - V_{BE})/R_B$.

The intersection of dc load line, with the output characteristics of calculated I_B is known as Q-point. This Q-point has been shown in fig (2).

NOTE: Definition of Q-point or Operating point.

"The Q-point is a point on load line which represents values of I_C and V_{CE} that exists in a transistor circuit when no input signal is applied." The best position of Q-point is middle of the load line.

Stability factor, S.

It is defined as "The rate of change of collector current I_C with respect to the reverse saturation current (I_{CO}) when both β and V_{BE} are constant". It is written as

$$S = \frac{dI_c}{dI_{co}} \mid \beta, \text{ and } V_{BE} \text{ are constant.}$$

Clearly, a low value of S offers a good thermal stability to the Q-point, i.e., for good thermal stability, S should be small. The stability factor 'S' is related to β.

Expression for stability factor,S:

In a Transistor the total collector current is given by

$$I_C = \beta I_B + (1+\beta) I_{CBO}$$

Differentiating this equation with respect to I_C (assuming β to be constant),

We get $\frac{dI_c}{dI_c} = \beta \frac{dI_B}{dI_c} + (1+\beta)\frac{dI_{CBO}}{dI_C}$

$$\Longrightarrow \quad 1 = \beta \frac{dI_B}{dI_c} + (1+\beta)\frac{1}{S}$$

$$\Longrightarrow \quad 1 - \beta \frac{dI_B}{dI_c} = (1+\beta)\frac{1}{S}$$

$$\Longrightarrow \quad S = \frac{(1+\beta)}{1-\beta\left(\frac{dI_B}{dI_c}\right)}$$

Thermal Runaway:

The flow of collector current, I_C produces heat within the transistor. This increases the transistor temperature and consequently the collector leakage current I_{CO}. Any increase in I_{CO} is magnified (1+β) times and increase the collector current I_C considerably, ($\because I_C = \beta I_B + (1+\beta)I_{CBO}$). This increased collector current further raises the transistor temperature that leads to further increase in I_{CO}. Hence, collector current again increases and the phenomenon is cumulative. Thus maximum collector current flows that exceed the limit and the transistor may be burnout.

"The self-destruction of an un-stabilized transistor is known as thermal runaway."

Transistor biasing arrangements:

As the CE circuit is most useful we shall consider the different biasing arrangements for this mode of operation only.

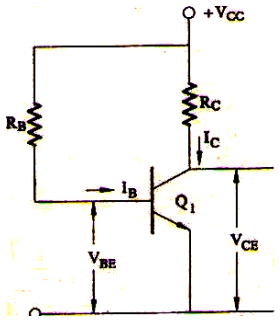
(i) Fixed bias: Fig (i) shows the fixed bias circuit. In this circuit, the quiescent base and collector currents are provided by a single power supply, V_{CC}. This keeps the E/B junction under forward bias and the collector base junction under reverse bias.

Applying KVL to the B/E loop, we get

V_{CC}-$I_B R_B$-V_{BE}=0

Or $I_B R_B$= V_{CC}-V_{BE}

∴ The base current $I_B = \frac{V_{cc} - V_{BE}}{R_B}$



Since V_{BE} is quite small (order of mV) as compared to V_{CC}. $I_B \approx \frac{V_{cc}}{R_B}$,

Here, I_B is independent of collector current I_C. Since the base current I_B is a constant the circuit is named as fixed-bias circuit.

Fig.(1) fixed bias circuit

Stability factor, S: It is given by $S = \frac{(1+\beta)}{1-\beta\left(\frac{dI_B}{dI_c}\right)}$

For fixed-bias circuit $\frac{dI_B}{dI_c} = 0$, ∴ S= (1+β)

Since β is always >50, the stability factor S is quite high. If β= 50, S=1+50 = 51. Therefore, it is rarely used.

Advantages: It is very simple circuit and it is very easy to fix operating point by simply changing the value of R_B.

Disadvantages: (1) The circuit does not provide a stable operating point (Q), thus the transistor gets destroyed by thermal runaway.

(2) If β changes due to transistor replacement, I_C (I_C = β I_B) also changes and hence the operating point shifts.

(ii.) Self Bias (Voltage divider Bias):

The self bias or voltage divider bias circuit is shown in fig (1). It provides a stable operating point and sufficient protection against thermal runaway. As shown in figure Fig.(1a) the resistors R_1, R_2, R_E & R_C and the supply voltage V_{CC} provide the proper FB to the E/B junction and proper RB to the C/B junction. The emitter resistor R_E provides thermal stabilization. Its stability factor is around 10. Hence it provides good thermal stability to the operating point. Thermal runaway is also prevented in this method of biasing. Hence it is also called as universal biasing method because it is used in almost all amplifier circuits.

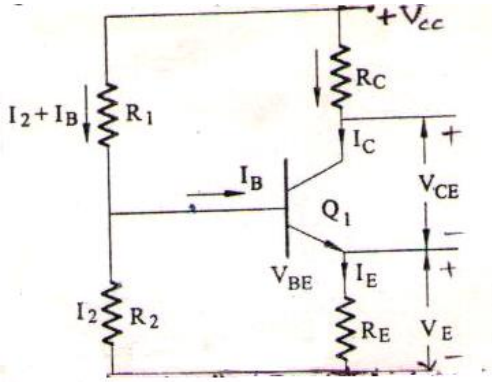


Fig.(1a) Voltage divider bias circuit

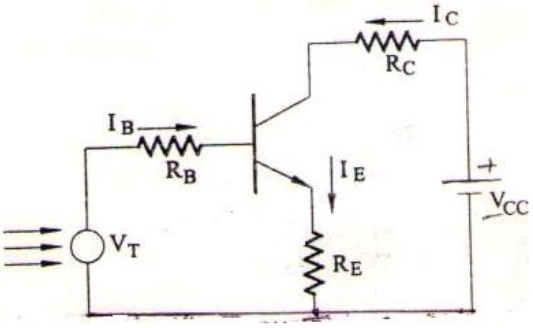


Fig.(1b) Thevenin's equivalent circuit.

Stabilization: "If the collector current I_C increases, due to increase in temperature, the voltage drop across R_E increases. This decreases V_{BE} leading to a decrease of I_B which, in turn, decreases the I_C to its original value"

Applying Thevenin's theorem the left of the terminals BG in fig (1) we get the voltage V_T and the effective base resistance R_B of the equivalent Thevenin's circuit and are given by

$$V_T = V_2 = V_{CC}\frac{R_2}{R_1+R_2}, \text{ and } R_B = \frac{R_1R_2}{R_1+R_2}$$

The equivalent circuit is shown in fig (2). Applying KVL to the input circuit of fig (2), we obtain

$$V_2 - I_BR_B - V_{BE} - I_ER_E = 0$$

$$\text{Or} \quad V_2 = I_BR_B + V_{BE} + (I_B + I_C)R_E \rightarrow (1) \quad [\because (I_B + I_C) = I_E]$$

Neglecting V_{BE} and solving for I_B we get

$$I_B = ((V_2 - I_CR_E)/(R_B + R_E))$$

Stability factor: Differentiating the equation

$$V_2 = I_B(R_B + R_E) + I_CR_E \rightarrow (2) \text{ [from equation (1), neglecting } V_{BE}]$$

Differentiating with respect to I_C, we have

$$0 = (R_B + R_E)\frac{dI_B}{dI_c} + R_E \quad [\because \frac{dV_2}{dI_c} = 0]$$

$$\frac{dI_B}{dI_c} = -\frac{R_E}{R_B+R_E} \rightarrow (3)$$

Substituting this value in expression for S, we have

$$S = \frac{(1+\beta)}{1+\beta R_E/(R_B+R_E)} \rightarrow (4)$$

$$= \frac{(1+\beta)(R_B+R_E)}{(R_B+R_E)+\beta R_E}$$

$$= \frac{(1+\beta)\,(1+\frac{R_B}{R_E})}{\frac{R_B}{R_E}+1+\beta} \rightarrow (5)$$

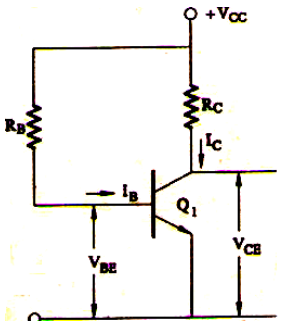
An examination of equation (5) shows S=1 when R_B/R_E is small and S= (1+β) when $R_B/R_E \rightarrow \alpha$, Thus, when R_B/R_E is small, S is equal to 1 and the circuit provides very good stability. Typical value of S is nearly 10.

Ex: 1 For the fixed bias arrangement shown in fig (1), V_{CC}= 12V, V_{CE} =2V, β=80 and I_C = 4mA. Calculate R_C and R_B.

Solution: From the output circuit, we can write

$$V_{CC} - I_CR_C - V_{CE} = 0$$

$$\therefore R_C = \frac{V_{CC}-V_{CE}}{I_c} = \frac{12-2}{4\times10^{-3}} = 2.5K\Omega$$



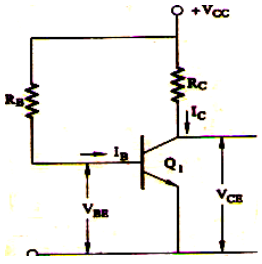
We have $I_C = \beta I_B \implies I_B = \frac{Ic}{\beta} = \frac{4\times10^{-3}}{80} = 50\mu A$

From input circuit $V_{CC} - I_BR_B - V_{BE} = 0$

$$\therefore R_B = \frac{V_{CC}-V_{BE}}{I_B} = \frac{12-0.7}{50\times10^{-6}} = \frac{11.3\times10^6}{50} = 226K\Omega$$

Ans: R_C= 2.5KΩ, R_B =226KΩ

Ex: 2. In a fixed bias circuit of fig (1), if β= 100, R_B= 200KΩ, R_C = 1KΩ and V_{CC} = 10V then find the values of I_C & V_{CE}.



Solution: To find I_B, $V_{CC} - I_BR_B - V_{BE} = 0$

$$\therefore I_B = \frac{V_{CC}-V_{BE}}{R_B} \approx \frac{V_{cc}}{R_B} = \frac{10}{200\times10^3} = 50\mu A$$

Collector current, $I_C = \beta I_B = 100 \times 50\mu A = 5mA$

From output current, $V_{CC} - I_C R_C - V_{CE} = 0 \Longrightarrow V_{CE} = V_{CC} - I_C R_C = 10 - 5 \times 10^{-3} \times 1 \times 10^3 = 10 - 5 = 5V$

$\therefore I_C = 5mA$ and $V_{CE} = 5V$

Ex: 3 A BJT used in Fig (1) has a $\beta = 49$, $V_{CE} = 7V$, $I_C = 4mA$, $R_C = 1.5K\Omega$ and $Vcc = 15V$. $R_1 \| R_2 = 1K\Omega$ and $R_E = 0.5K\Omega$. Evaluate stability factor 'S'. Also corresponding change in I_C if $\Delta I_{CO} = 20$ nA

Solution: we have, $S = \frac{(1+\beta)\left[1+\frac{R_B}{R_E}\right]}{1+\beta+\frac{R_B}{R_E}} = (1+49)\left(1+\frac{1}{0.5}\right) / 1 + 49 + \frac{1}{0,5} = \frac{50(3)}{53} = \frac{150}{53} = 2.8$

If $\Delta I_{CO} = 20$ nA, then $\Delta I_C = S \times \Delta I_{CO} = 2.8 \times 20 \times 10^{-9} = 56nA = 0.056\mu A$

Ex: 4 Find the Q-point for the circuit shown in fig (1) if $V_{BE} = 0.5V$ and $\beta = 40$

Solution: Open circuit voltage across A, B is $V_{R_2} = \frac{R_2}{R_1+R_2}.V_{CC} = V_{OC} = \frac{4\times10^3}{(40+4)\times10^3} \times 22 = 2V$

$\therefore$ From input circuit $V_{OC} - V_{BE} - I_E R_E = 0$ (Or) $V_{OC} - V_{BE} - I_C R_E = 0$ [$\because I_C \cong I_E$]

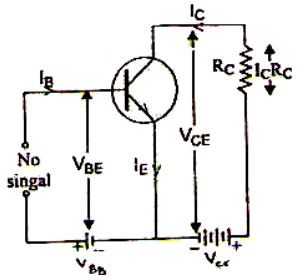
$\therefore I_C = \frac{V_{OC}-V_{BE}}{R_E} = \frac{2-0.5}{1.5\times10^3} = 1mA$

Then $V_{CE} = V_{CC} - I_C R_C - I_E R_E = V_{CC} - I_C (R_C + R_E)$ [$\because I_C \cong I_E$]

$= 22 - 1\times 10^{-3}(10+1.5)\times 10^3$

$= 22 - 11.5 = 10.5V$

$\therefore$ Q-Point is (1mA, 10.5V)



Ex: 5 In the circuit diagram shown in Fig (1), $V_{CC} = 12V$ & $R_C = 6K\Omega$. Draw dc load line. What will be Q-Point of zero signal base current is $20\mu A$ and $\beta = 50$.

Solution: $V_{CE} = V_{CC} - I_C R_C$

When $I_C = 0$, $V_{CE} = V_{CC} = 12V \longrightarrow$ Point A

When $V_{CE} = 0$, $I_C = \frac{V_{CC}}{R_C} = \frac{12}{6\times10^3} = 2mA \longrightarrow$ Point B

Joining points A & B, dc load line is obtained. At zero signal, $I_B = 20\mu A$

$= 0.02mA$

$I_C = \beta I_B = 50 \times 0.02 = 1mA$, $V_{CE} = V_{CC} - I_C R_C = 12 - 1 \times 10^{-3} \times 6 \times 10^3 = 12 - 6 = 6V$

$\therefore$ Co-ordinates of Q-Point are 6V, 1mA.

FIELD EFFECT TRANSISTORS (FETs)

Introduction:

FET is a 3 terminal device, since the electric field controls the conduction process, they are called field effect transistors.

FET is a unipolar device i.e., its operation depends only on one type of charge carriers either electrons or holes.

Types of FETs: There are two main categories of FETs:

(1) Junction Field Effect Transistors (JFETs) [(i) N-channel JFETs & (ii) P-channel JFETs]

(2) Insulated Gate FET (IGFET) / Metal Oxide Semiconductor FET (MOSFET/ MOST)

MOSFET is further subdivided into two types

(i) Depletion and Enhancement MOSFET (DE-MOSFET or D-MOSFET)

(ii) Enhancement only MOSFET (E-only MOSFET or E-MOSFET).

Differences between FET and BJT.

1. FET is a unipolar device whereas BJT is a bipolar device.
2. FET exhibits a very high input resistance (order of several 100 of $M\Omega$) whereas BJT has input resistance in several $K\Omega$.
3. FET is voltage controlled device whereas BJT is a current controlled device.
4. FET is simpler to fabricate than BJT.
5. FET has better thermal stability than BJT.
6. FET is less noisy than a BJT. And
7. The main disadvantage of FET is its relatively low gain bandwidth product in comparison to BJT.

JFET construction**:**

Fig (1) shows the construction of junction Field Effect Transistor. It consists of a bar of N-type or P-type semiconductor with ohmic contacts at the two ends. One end is called source (S) and the other end is drain (D). The bar acts as a simple resistor. The region of oppositively doped semi conducting material diffused around the bar constitutes the third element, called gate (G). The region of N-type or P-type between the two depletion regions is called channel.

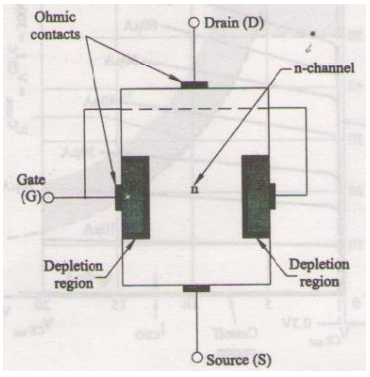


Fig (1) constructional features

The junction FET has two p-n junctions. The result is a depletion region at each junction. Depletion regions shown in Fig (1) are under no bias condition. The majority charge carriers (for N-channel JFET electrons/ for P-channel JFET holes) enter the channel through the source (S) and they leave the bar

through the drain (D). The charge carriers flow through the channel and are controlled by the terminal called the gate (G).

Circuit symbols of JFETs:

The circuit symbol for N-channel and P-channel JFETs are shown in Fig (1) (a) and (b) respectively. The vertical line in the symbol represents the channel to which source(S) and drain (D) are connected.

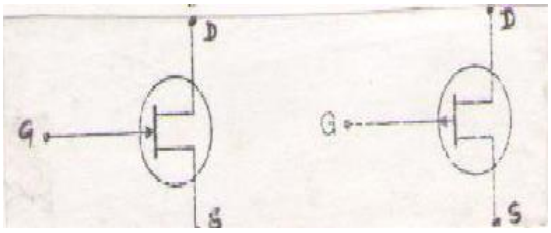
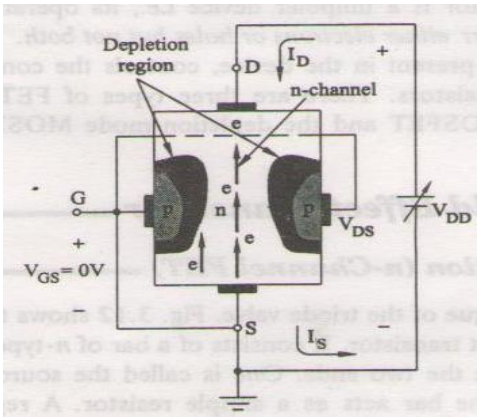
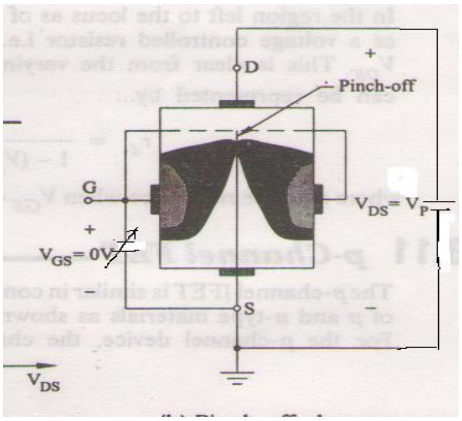


Fig (1.a) N-channel Fig (1.b) P-channel

Working of JFET: Consider an N-channel JFET to explain its working (or operation) as shown in fig (1), under different operating conditions.



Fig(1) n-channel FET



Fig(2) Pinch-off phenomenon

(i) When V_{GS} = 0 V and V_{DS} = 0V. When no voltage is applied between drain and source, & gate and source, the thickness of the depletion regions around the PN junctions is uniform as shown in fig(1).

(ii) When $V_{GS} < 0$ and $V_{DS} = 0$. In this case, the PN junctions are reverse biased. So, as V_{GS} decreased from zero, the reverse bias voltage across the PN junction is increased and hence, the thickness of the depletion region in the channel increases until the two depletion regions make a contact with each other. In this condition, the channel is said to be cut-off. The value of V_{GS} which is required to cut-off the channel is called the cut-off voltage, V_P in Fig (2).

(iii) When V_{GS} = 0 and $V_{DS} > 0$V. Drain is positive with respect to the source with V_{GS} = 0. Now the majority charge carriers (electrons) flow through the N-channel from S to D. Therefore, the conventional current I_D flows from drain to source.

As V_{DS} is increased, the width of the channel will be reduced. At a certain value V_P of V_D, the width of the channel at 'B' becomes minimum. At this voltage, the channel is said to be pinched-off and the drain voltage V_P is called the pinch-off voltage.

Experimental Arrangement to Obtain Output / Drain Characteristics

Fig (1) shows the circuit diagram for determine the output / drain characteristics and transfer / trnasconductance characteristics given JFET, where V_{GS} is the gate supply voltage and V_{DD} is the drain supply voltage sources.

1. Output / Drain characteristics: The curves obtained by plotting drain current I_D and drain to source voltage (V_{DS}) for fixed gate source voltage (V_{GS}) is called the drain characteristics.

Keeping V_{GS} fixed at some value, the V_{DS} is changed in steps and corresponding I_D is noted.

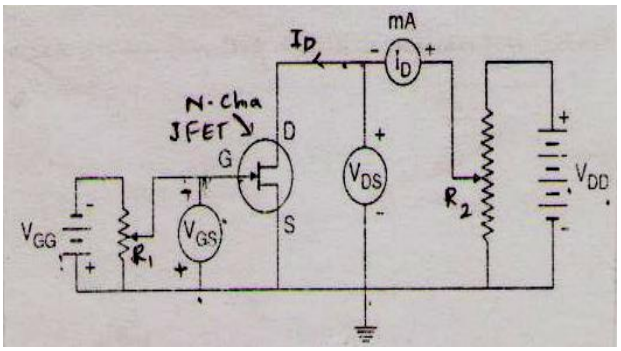


Fig (1) Circuit arrangement

A group of such drain characteristics curves are drawn by setting V_{GS} at different fixed values. Fig (2) shows a family of drain characteristics. The following points may be noted from the drain characteristics.

(i) For low values of V_{DS} ($<V_P$), the drain current I_D varies directly with voltage following ohms law.

Thus the region between 0 and P is called ohmic region and the JFET behaves like an ordinary resistor.

This is useful as a voltage variable resistor (VVR) /voltage dependent resistor (VDR).

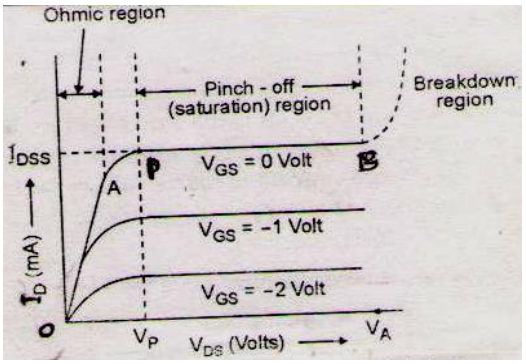


Fig (2)

(ii) As V_{DS} is increased beyond V_P, the I_D becomes maximum and constant. The V_{DS} at which I_D becomes constant is called the pinch-off voltage, V_P. The region between P and B is called the saturation or pinch-off region.

(iii) When $V_{DS} = V_P$, I_D becomes maximum, known as I_{DSS} when $V_{GS} = 0V$.

(iv) If V_{DS} is increased beyond breakdown voltage point, I_D suddenly increases and JFET enters the breakdown region due to avalanche multiplication of electrons in the depletion region between gate and drain.

(2) Transfer / Transconductance characteristics:

It is plot of I_D versus V_{GS} for a foxed value of V_{DS} as Shown in fig (3).

To get the characteristics, V_{DS} is kept fixed while V_{GS} is varied in steps and the corresponding I_D is noted.

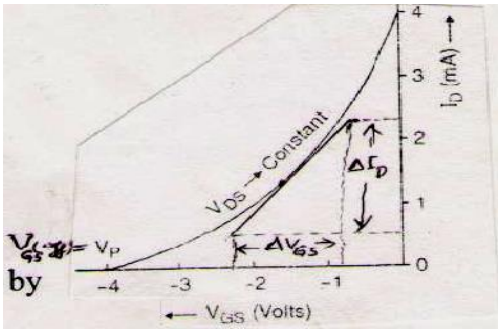


Fig.(3)

It is seen from the characteristics of fig (3), when V_{GS} = 0, I_{DS} = I_{DSS} and when I_D = 0, V_{GS} = V_P. or $V_{GS(off)}$ .This characteristics curve follows the Shockley's equation given by

$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$, where I_{DSS} and V_P are constant for a particular / given JFET.

In a JFET, the drain current I_D depends upon the voltages V_{DS} and V_{GS}. Any one of these variables may be fixed and the relations between the other two are determined. These relations are determined by the 3 parameters, called mutual / transconducatnce (g_m), drain resistance (r_d) and the amplification factor (μ).

(i) Mutual / Transconducatnce, (g_m).

It is defined as the ratio the ratio of a small change in the drain current, (ΔI_D) to the corresponding small change in the gate voltage (ΔV_{GS})." The unit of the g_m is mho or siemens

It is the slope of the transfer characteristics curve, and given by

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$, V_{DS} is held constant.

(ii) Drain resistance, (r_d).

It is defined as the ratio of a small change in the drain voltage (ΔV_{DS}) to the corresponding small change in the drain current at a constant gate voltage. The unit of drain resistance, r_d is ohms.

It is the reciprocal of the slope of the drain characteristics and is given by

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D}$$, V_{GS} is held constant.

Note**: T**he reciprocal of the drain resistance is called the drain conductance, $g_d = 1/r_d$.

(iii) Amplification factor, **(** μ) :

It is defined as the ratio of small change in the drain voltage, ΔV_{DS} to the corresponding small change in the gate voltage, ΔV_{GS} , at a constant drain current I_D. It is given by

$$\mu = -\frac{\Delta V_{DS}}{\Delta V_{GS}}$$, I_D is constant.

Note: Here, the –ve sign indicates that when V_{GS} is increased, V_{DS} must be decreased for I_D to remain constant.

Typical values of r_d = 10KΩ to 100KΩ ; μ = 0.1 to 20

Relation between FET parameters:

From the definition of the amplification factor μ is given by $\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} = \frac{\Delta V_{DS}}{\Delta I_D}\frac{\Delta I_D}{\Delta V_{GS}}$

Now from the definitions of r_d and g_m, $r_d = \Delta V_{DS}/\Delta I_D$ and $g_m = \Delta I_D/\Delta V_{GS}$

$$\therefore \quad \mu = r_d . g_m$$

Mathematical expression for g_m:

According to Shockley equation, $I_D = I_{DSS}\left[1-\frac{V_{GS}}{V_P}\right]^2 \rightarrow (1)$

Differentiating the equation (1) w.r.t. V_{GS}, we have $\frac{dI_D}{dV_{GS}} = 2 I_{DSS}\left[1-\frac{V_{GS}}{V_P}\right](-\frac{1}{V_P})$

$$g_m = \frac{-2I_{DSS}}{V_P}\left(1-\frac{V_{GS}}{V_P}\right) \rightarrow (2)$$

Let, when $V_{GS} = 0$, $g_m = g_{mo} \quad \therefore g_{mo} = \frac{-2I_{DSS}}{V_P} \rightarrow (3)$

From equations (2) & (3), we get $g_m = g_{mo}\left(1-\frac{V_{GS}}{V_P}\right)$

Applications of FET:

1. FETs are used in electronic voltmeters, since it has very high input impedance and hence draws no current.
2. FET is used as an excellent buffer amplifier in measuring instruments, receivers etc., since high input impedance and low output impedance.
3. FETs are used in digital circuits in computers, memory circuits because of its small size.
4. FETs are used in RF amplifiers in FM tuners and communication equipment for the low noise level.
5. FET is used as a voltage variable resistor (VVR or VDR) in tone controls since it is a voltage controlled device.

FET as a voltage variable resistor (VVR):

In the ohmic region (i.e., before pinch-off region), where V_{DS} is small (< V_P), the drain to source resistance r_d can be controlled by the bias voltage V_{GS}.

In FET, the drain-to-source conductance, $g_d = \Delta I_D/\Delta V_{GS}$. For small values of V_{DS}, it may also be written as $g_d = g_{do}\left(1-\left(\frac{V_{GS}}{V_P}\right)^{\frac{1}{2}}\right)$, where g_{do} is the value of drain conductance when V_{GS} =0.

The variation of the r_d with V_{GS} can be closely approximated by an expression

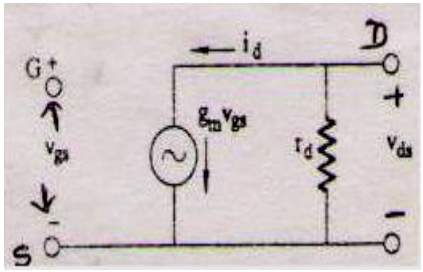
$r_d = r_o/1-KV_{GS}$ where r_o is the value of the drain resistance at V_{GS} =0, and K= a constant, dependent upon FET type.

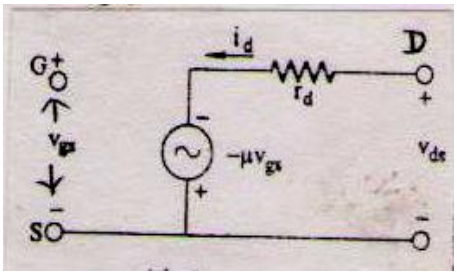
Thus, small signal FET drain resistance r_d varies with V_{GS} and FET acts like a variable passive resistor.

FET finds wide applications where VVR property is useful. For example the VVR can be used in Automatic gain control (AGC) of multi stage amplifier.

AC equivalent circuit of FET: The drain current I_D is a function of V_{GS} and V_{DS}. Therefore, the ac component of i_d can be expressed as $i_d = g_m v_{gs} + v_{ds} / r_d \rightarrow (1)$ Equation (1) may be written as $v_{ds} = i_d r_d - \mu v_{gs} \rightarrow (2)$.

Based on the equations (1) and (2), two equivalent circuits of FET may be drawn, Fig(1).





Fig(1) Small signal JFET models (a) (b)

MOSFETs (IGFETs)

(I) Depletion MOSFET (DMOSFET or DEMOSFET):

Construction: The construction of N-channel Depletion MOSFET is shown in fig (1). In this,two heavily doped n^+ regions are diffused into p-type substrate, to serve as the source (S) and the drain (D). An N-type channel is diffused between the S and D. A thin insulating layer of SiO_2 is grown over the surface of the structure, and holes are cut in to the SiO_2 layer, allowing contact with S and D. Then metal contacts are made to the S, D and gate G. The metal gateG, P-type substrate and SiO_2 layer between them together form a parallel plate capacitor. This insulating layer gives extremely high input impedance (order of 10^9 MΩ) for the DMOSFET.

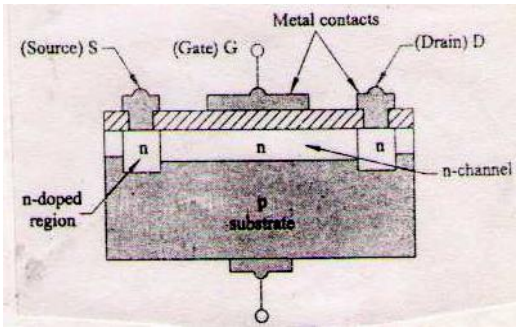
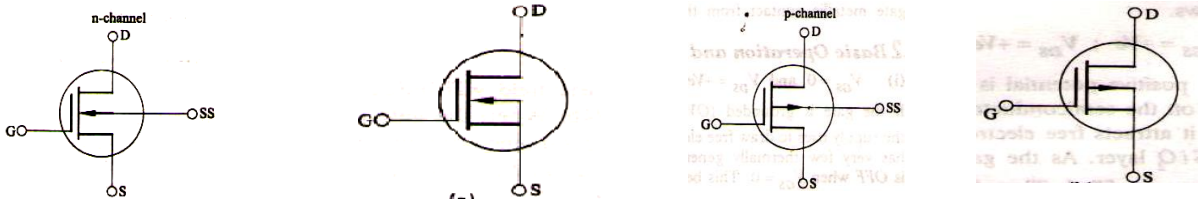


Fig (1) n-channel Depletion type MOSFET

Circuit symbols of DMOSFET: The circuit symbols for an N-channel and P-channel DMOSFETs are shown in fig (2).



(a) N-channel DMOSFET (b) P-channel DMOSFET

Fig. (2)

Working of DMOSFET: Fig 3 (a) and (b) shows the biasing voltages to explain its working.

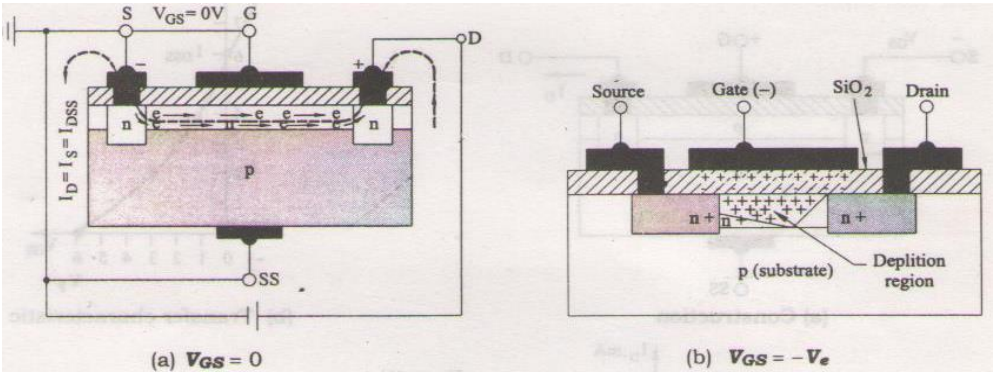


Fig (3) Depletion MOSFET

(i) When V_{GS} = 0 V and V_{DS} at +ve voltage, free electrons in the N-channel are attracted by the potential at the drain (D). This behavior is similar to that of the JFET. The saturation current under this condition is labeled as I_{DSS} i.e., drain current with V_{GS} = 0 V.

(ii) When V_{GS} at +ve voltage and V_{DS} at +ve voltage, electrons are induced into the channel through the gate capacitor, makes the channel more conductive i.e., decreases channel résistance and drain current I_D increases as V_{GS} is made more +ve , then the MOSFET is said to be in enhancement mode.

(iii) When V_{GS} is at –ve voltage and V_{DS} at +ve voltage, +ve charges are induced in the channel through the gate capacitor. The induced +ve charges in the channel makes it less conductive and drain current, I_D decreases as V_{GS} is made more -ve . The redistribution of charge in the channel causes a depletion layer, hence the name depletion MOSFET. As shown in fig 3(b), because of the voltage drop due to the drain current, the channel width is narrow near the drain. This is similar to the pinch-off occurring in JFET..

Characteristics of DMOSFET.

(i) Drain characteristics: **D**rain characteristics curves for N-channel DMOSFET is shown in fig (4).

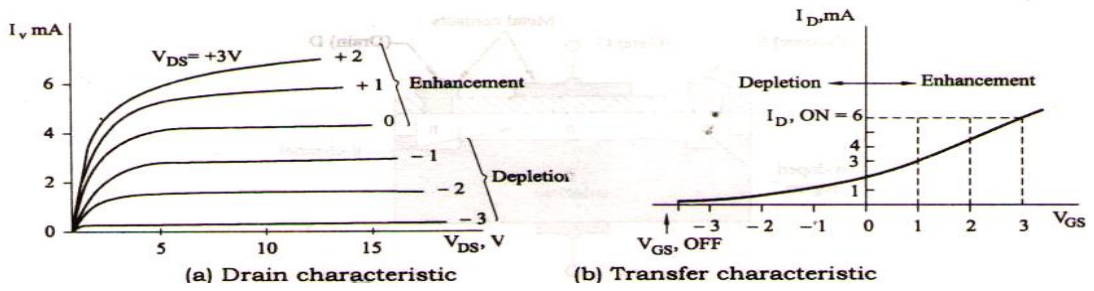
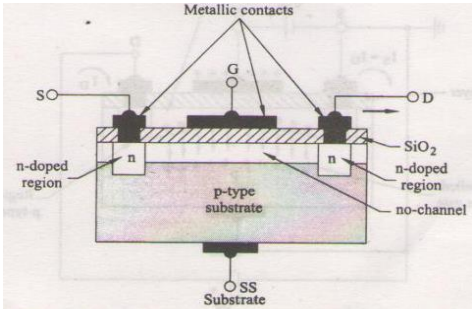


Fig.(4) N-channel Depletion MOSFET characteristics.

It is seen that N-channel DMOSFET can be operated in either the enhancement mode or the depletion mode, as shown in fig (a). The enhancement mode occurs for +ve values of V_{GS} while the depletion mode occurs for negative values of V_{GS}.

(ii) Transfer characteristics: The transfer characteristic curve of an N-channel DMOSFET is shown in fig (5). It is seen that drain current I_D flows even when gate-bias V_{GS}=0. When V_{GS} is made more and more –ve, I_D goes on decreasing.



(II) Enhancement MOSFET (EMOSFET):

Construction: The construction of N-channel EMOSFET is shown in Fig (1). In this two heavily n^+ regions are diffused into the P-type substrate, to serve as the source (S) and the drain (D). A thin insulating layer of SiO_2 is grown over the surface of the structure and holes are cut into the SiO_2 layer but still it is termed as N-channel EMOSFET because the thin layer of P-substrate touching the SiO_2 layer provides channel for electrons, called induced N-channel, hence the name N-channel EMOSFET.

Fig(1)

Circuit symbols of EMOSFET: The circuit symbols for an N-channel EMOSFET and P-channel EMOSFET are shown in fig (2).

(a) N-channel EMOSFET. (b) P-channel EMOSFET

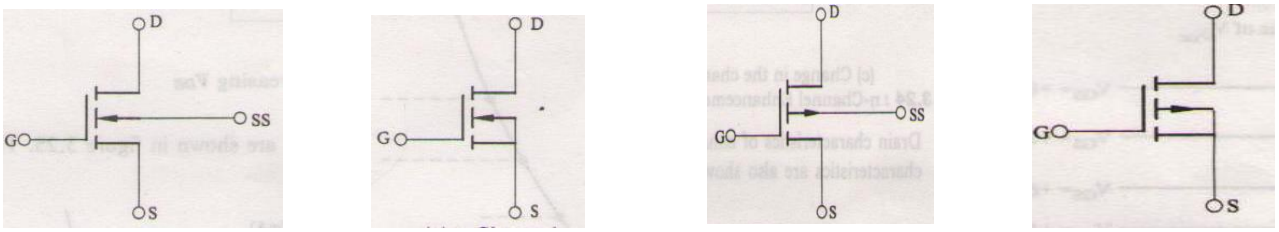


Fig. (2) Circuit Symbols of Depletion MOSFETs

Working of EMOSFET:

(i). V_{GS} = 0 & V_{DS} = +ve V.

If the gate is grounded (0V) and when some +ve voltage is applied to the drain, the supplytries to draw free electrons i.e., minority carriers in P-substrate. As a result, this type ofMOSFET is OFF when V_{GS} = 0. This behavior of EMOSFET is different from that of the DMOSFET and JFET where I_{DSS} flows.

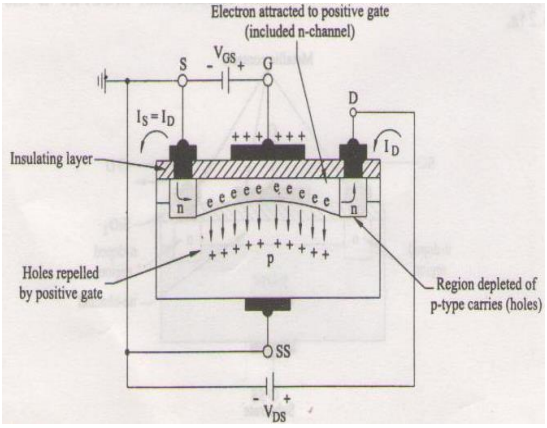


Fig.(3)

(ii) V_{GS} = +ve V & V_{DS} = +ve V.

When a positive voltage is applied to the gate G w.r.t. source to which P-substrate is also connected [Fig (3)], the capacitor begins to charge. As the gate voltage is further increased, negative charges (electrons) appear in the substrate between the drain and source. This layer between S and D is called the N-type inversion layer or induced n-channel. Due to N-channel, the device will be ON and electrons flow from the drain to the source.

The value of V_{GS} voltage that causes significant increase in drain current is called the threshold voltage, V_T. When $V_{GS} < V_T$, $I_D = 0$. When $V_{GS} > V_T$, N-channel exists between S and D and the drain current increases.

If we keep V_{GS} constant and increase the drain voltage, the I_D eventually reaches a saturation value as in DMOSFET and JFET. The saturation of I_D is caused by the pinching-off process shown in fig (4).

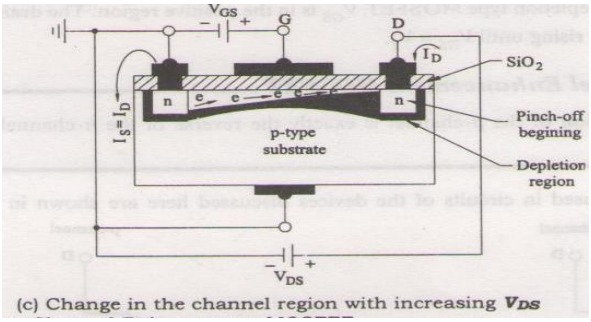


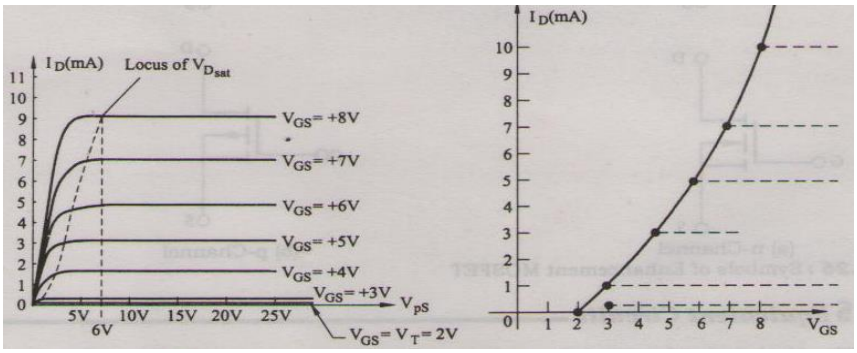
Fig (4) n-channel Enhancement MOSFET

Characteristics of EMOSFET:

(i) Output (or) Drain characteristics:

Drain characteristic curves for N-channel MOSFET is shown in fig (5).

Each characteristic shows the variation of drain current I_D with the V_{DS} for a fixed value of V_{GS}.



Fig(5) (a) Drain characteristics (b) Transfer characteristics

The following points may be noted from the characteristics:

(i) For values of V_{GS} less than the threshold voltage V_T, the drain current is zero.

(ii) As V_{GS} is increased from V_T (=V_{GS} =2V), the saturation level also increases from 0 to10mA.

(iii) The spacing between levels of V_{GS} increases as the value of V_{GS} increases.

Transfer characteristics: The transfer characteristic curve of an N-channel E-MOSFET is shown in fig (6). It is seen from the characteristics that the drain current does not start rising until V_{GS} = or > threshold voltage, V_T. With increase in V_{GS}, I_D increases slowly at first and then rapidly (as shown in fig (6).

SHORT NOTES & PROBLEMS

1Q. what are shorted-gate drain current (I_{DSS}), Pinch-off voltage (V_P) and gate-source cut-off voltage. ($V_{GS(off)}$) and threshold voltage.

(i) I_{DSS}: The drain current with shorted-circuited to gate ($V_{GS} = 0$) and drain source voltage (V_{DS}) equal to pinch-off voltage (V_P) is called I_{DSS}.

(ii) Pinch-off voltage,(V_P): The minimum drain-source voltage(V_{DS}) at which the drain current (I_D) reaches constant maximum value is called pinch-off voltage.

(iii) V_T: The value of V_{GS} voltage that causes significant increase in drain current, I_D is called the threshold voltage (V_T).

(iv) $V_{GS\ (oFF)}$: The minimum gate-source voltage,(V_{GS}) at which the channel is completely cut-off and the drain current (I_D) becomes zero is called $V_{GS(OFF)}$

2Q. what are advantages of FET over BJT.

(i) It has high input impedance (order of $M\Omega$)

(ii) It has low output impedance (order of Ω)

(iii) Low noise level (iv) Low offset voltage (v) Simpler to fabricate.

(vi) It occupies less space in integrated circuits.

3Q. State the differences between JFET and MOSFET.

(i) MOSFETs have very high impedance (order of 10 to $10M\Omega$) than that of JFET

(ii) Inter electrode capacitances of MOSFETs independent of bias voltage in MOSFETs than in the case of JFET.

(iii) MOSFETs are simpler to fabricate than that of JFET.

4Q. Mention the applications of MSOFETs

(i) Because of very high input impedance of the order $10^{15}\ \Omega$, they are used in voltmeters, called FET input voltmeters.

(ii) Because of their high input resistances, the MOSFETs have been used as micro-resistors in ICs.

(iii) MOSFETs are easy to fabricate, therefore they are widely used in digital ICs.

PROBLEMS

1. Following readings were obtained experimentally for FET .Determine the parameters of the FET.

V_{GS}	- 0 V	-0V	- 0.3V
V_{DS}	5V	10V	10V
I_D	8mA	8.2mA	7.6mA

Solution: (i) With V_{GS} constant at 0V,

ΔV_{DS} = 10 – 5 = 5V, ΔI_D =8.2 – 8 = 0.2mA $\therefore$ $r_d = \dfrac{\Delta V_{DS}}{\Delta I_D} = \dfrac{5V}{0.2mA} = 25K\Omega$

(ii) With V_{DS} constant, at 10 V, ΔV_{GS} = 0.3 - 0 = 0.3V, ΔI_D =8.2 – 7.6 = 2mA

$$\therefore \quad g_m = \Delta I_D / \Delta V_{GS} = 0.6mA/0.3V = 3\text{mS}$$

(iii) $\mu = g_m r_d = (25\times10^3)\times(2\times10^{-3}) = 50$

2. An N-channel JFET has V_P = -4.5V and I_{DSS} =9mA. At what value of V_{GS} in the pinch-off region will I_D equal to 3mA?

Solution: $I_D = I_{DSS}\left[1-\dfrac{V_{GS}}{V_P}\right]^2 \Rightarrow 3 = 9\left(1-\dfrac{V_{GS}}{-4.5)}\right)^2$ or $\dfrac{3}{9} = \left(1+\dfrac{V_{GS}}{4.5}\right)^2$

or $1+\dfrac{V_{GS}}{4.5} = \dfrac{1.732}{3} = 0.577$

$V_{GS}/4.5 = 0.577 - 1 = -0.423 \Rightarrow V_{GS} = -4.5\times0.423 = -1.9V$

3. For N-channel JFET, find I_D, g_{mo}, & g_m if I_{DSS} = 6.3mA, V_P =-3V, V_{GS} = -1V.

Solution: We have $I_D = I_{DSS}\left[1-\dfrac{V_{GS}}{V_P}\right]^2 = 6.3\times10^{-3}\left(1-\dfrac{(-1)}{(-3)}\right)^2 = 6.3\times10^{-3}\,(1\text{-}0.333)^2$

$= 6.3\times10^{-3}\,(0.666)^2 = 6.3\times10^{-3}\times 0.44 = 2.8\text{mA}.$

(ii) When V_{GS} =0, $g_m = g_{mo}$,

$\therefore g_{mo} = -\dfrac{2I_{DSS}}{V_P} = -\dfrac{2\times6.3\times10^{-3}}{-3} = \dfrac{12.6\times10^{-3}}{3} = 4.2\text{mS}$

(iii) $g_m = g_{mo}\left(1-\dfrac{V_{GS}}{V_P}\right) = 4.2\times10^{-3}\left(1-\dfrac{(-1)}{(-3)}\right) = 4.2\times10^{-3}\,(1\text{-}0.333) = 4.2\times10^{-3}\,(0.666)$

$= 2.8\text{mS}$

UNIJUNCTION TRANSISTOR

Introduction:

Basically, UJT is a three-terminal silicon diode. As its name indicates, it has one p-n junction. It differs from an ordinary diode in that it has three leads and it differs from a FET in that it has no ability to amplify. However, it has ability to control a large power with a small signal. It also exhibits negative resistance characteristics which makes it useful as an oscillator.

Construction:

The construction of a UJT is similar to that of a FET. Its basic structure is shown in fig (1). It consists of a lightly doped silicon bar acts as a base and a heavily doped P-type impurity is added to its one end (closer to B_2) to get a single p-n junction. As shown in fig (1) there are three terminals: emitter (E) and two bases B_1 and B_2 at the top and bottom of the silicon bar. Since the two base terminals are taken from one section of the diode, this device is called as double-base diode.

The p-region (emitter) is heavily doped having many holes. However, the N-region is lightly doped. Hence if the emitter is open, the resistance between the base terminals $B_1$and B_2 is very high (5KΩ to10 KΩ).

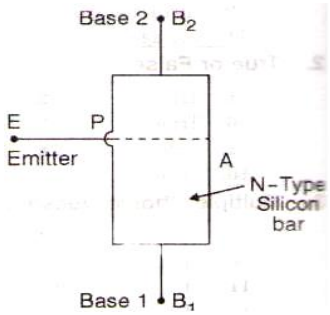


Fig (1)

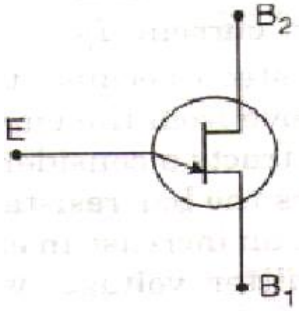


Fig (2)

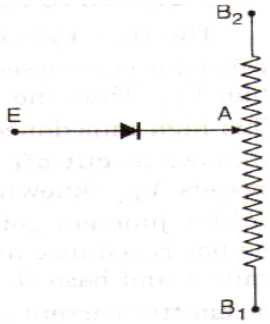


Fig (3)

Circuit Symbol of UJT:

The circuit symbol of a UJT is shown in fig (2).The emitter leg is drawn at an angle to the vertical line and arrow points in the direction of conventional current when UJT is in the conducting state.

Equivalent circuit of UJT

The equivalent circuit is shown in fig (3). The point A denotes the point where P region is formed. The point A is such that $R_{B1} \rangle R_{B2}$ where y R_{B1} and R_{B2} denote the resistances of silicon bar between $B_1$and A, and A and B_2 respectively. Usually R_{B1} = 60% of R_{BB} where $R_{BB} = R_{B1} + R_{B2}$

Interbase resistance of UJT:

It is the resistance between $B_1$and B_2 i.e., the total resistance of the silicon bar from one end to the other end with emitter terminal is open. i.e., $R_{BB} = R_{B1} + R_{B2}$.

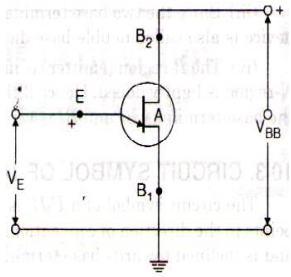


Fig (4)

Intrinsic Stand- Off Ratio of UJT: From the figure (3), it is seen that emitter acts as a voltage divider tap on the fixed resistance R_{BB}. The voltage division factor is given a special symbol (η) and is called "**intrinsic stand off ratio".**

It is given by $\eta = \dfrac{R_{B1}}{R_{B1}+R_{B2}} = \dfrac{R_{B1}}{R_{BB}}$

Operation of UJT:

The operation of the UJT can be explained using thefigure as shown in fig (4). Generally the base1 (B_1) is grounded and a positive voltage V_{BB} is applied to base 2 (B_2). When there is no emitter current, this voltage (V_{BB}) produces a uniform voltage across the silicon bar. Now the voltage drop developed across the R_{B1} is (A&B_1), $V_A = V_{BB}\dfrac{R_{B1}}{R_{B1}+R_{B2}} = \eta V_{BB}$ where $\eta = \dfrac{R_{B1}}{R_{B1}+R_{B2}} = \dfrac{R_{B1}}{R_{BB}}$.

Now the voltage applied between emitter and base1, V_E is less than V_A+V_B (V_B = barrier voltage of Jn) the p-n junction is reverse biased and only a very small reverse current,(I_E) flows in the emitter circuit.

Now the voltage applied between emitter and base1,V_E is less than $V_A + V_B$ (V_B = barrier voltage of the Jn) the p-n junction is reverse biased and only a very small reverse current,(I_E) flows in the emitter circuit.

When emitter voltage V_E exceeds the peak point voltage, V_P (= $V_A + V_B = \eta V_{BB} + V_B$)

the junction forward biased and the emitter current I_E increases. Then the UJT is said to have been fired or turned ON. Consequently the resistance R_{B1} decreases and the emitter voltage suddenly decrease and reaches to a minimum value, is called valley voltage V_V. Since emitter voltage decreases when emitter current increases, the UJT possesses negative resistance.

Characteristics of UJT:

The UJT emitter characteristic for a given interbase voltage V_{BB} is shown in fig (1). The characteristic is divided into three regions called cut off region, -ve resistance region and saturation region as shown in fig (1).

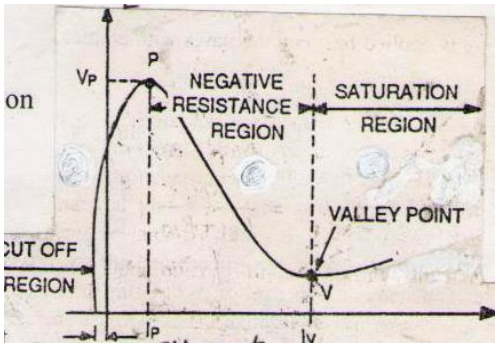


Fig (1) V-I characteristics

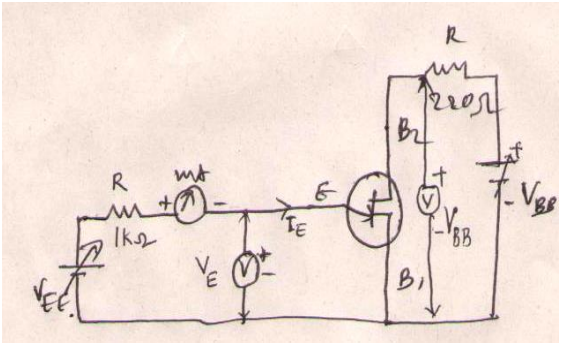
Cut off region: In this region, the UJT is reverse biased until the emitter voltage is less than V_P. Thus the device is in the OFF state. This region is shown in fig (1) by the region (1) and is called cut off region.

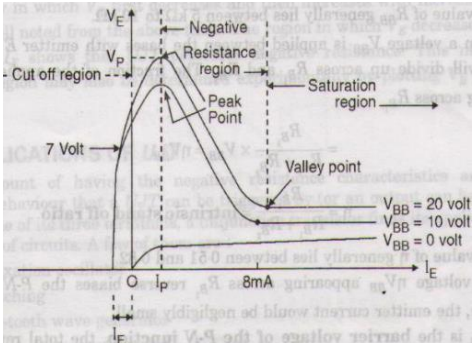
Negative resistance region: When the emitter voltage exceeds the V_P (firing voltage), the emitter junction gets forward biased so that the bar resistance and hence voltage between emitter, E and base (B_1) drops to a low value and the emitter current I_E rises considerably. Thus the device shows -ve resistance region in its V-I characteristic and is shown by the region (2).

Saturation region: When the value of current exceeds I_V, the voltage between emitter and base B_1 begins to rise again. The UJT is now in the ON state and is shown in by the region (3), is called the saturation region.

Experimental Arrangement To Draw Emitter Characteristic And Determination Of UJT Parameters.

Circuit description: Experimental arrangement to draw the emitter characteristic is shown in below fig (1). As shown in figure the base terminal B_1 is grounded. A variable emitter supply voltage, V_{EE} is connected between emitter and base B_1 and a variable base supply voltage V_{BB} is connected between the terminals base B_1 and B_2. A milliammeter is connected in the emitter circuit to read the emitter current, I_E. Two voltmeters are connected in the circuit to measure the emitter voltage, V_E and inter base voltage, V_{BB}.





Procedure: **Fig(1) ckt arrangement** **Fig(2) Emitter characteristics**

Keeping V_{BB} fixed at some value, the emitter voltage (V_E) is changed in equal steps and the corresponding emitter current (I_E) is noted. A family of such emitter characteristics is drawn by setting V_{BB} at different fixed values. Fig (2) shows a family of UJT emitter characteristics.

The following points may be noted from the characteristics.

(i) At beginning the UJT is reverse biased and hence no current flows in the circuit as shown in Fig (2).

(ii) When the emitter voltage exceeds the V_P, then the UJT becomes forward biased and conducts heavily. Consequently voltage decreases to a minimum value (valley voltage) and current increases sharply as shown in fig (2). This region is called negative resistance region because voltage is decreasing, and current is increasing.

Determination of UJT parameters:

Intrinsic Stand off ratio (η)

From the emitter characteristics, note the value of peak point voltage, V_P for a fixed value of V_{BB}. Now the value of η can be determined using the relation $\eta = (V_P - V_B)/V_{BB}$, where V_B barrier voltage of the P-n junction and is 0.7V for silicon

R_{B1} and R_{B2} : Measure the value of R_{BB}, i.e. the resistance between B_1 and B_2 (when emitter is open) using a multi-meter. Now, we can determine $R_{B1} = \eta R_{BB}$ and $R_{B2} = R_{BB} - R_{B1}$.

Peak point emitter current, I_P.

The emitter current, I_E corresponding to the peak point voltage is called peak point emitter current, I_P. It represents the minimum current that is required to trigger the device.

Valley point voltage V_V and valley point current I_V:

The emitter voltage at the valley point is called V_V and the corresponding valley point current I_V is noted from the emitter characteristics.

Applications:

Because of its negative resistance characteristic, it can be used in a variety of applications.

(1) Relaxation oscillator (2). Switching circuits (3) Saw-tooth wave generator (4).Sine wave generator (5). Timing and trigger circuits (6).Voltage or current regulated supplies (7).Phase control.

UJT as Relaxation Oscillator:

Relaxation oscillator using an UJT is shown if fig (1).It consists of a UJT and a capacitor 'C' which is charged through 'R' when V_{BB} is switched on. Initially the capacitor 'C' is uncharged

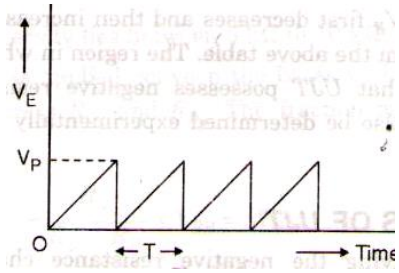
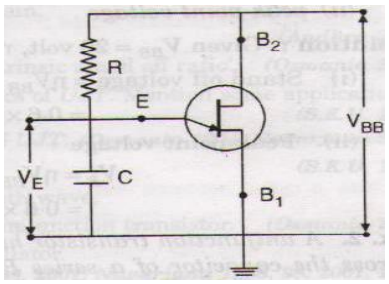


Fig (2) Saw tooth wave



Fig(1) Relaxation oscillator

and emitter voltage V_E is zero. The capacitor 'C' starts Charging through "R' due to the presence of V_{BB} and continues to do so till the emitter voltage rises to V_P, the firing potential. The capacitor discharges quickly through R_{B1} so that UJT returns to OFF state to restart the cycle.

If the capacitor takes a time T to charge to firing potential V_P,

Then $V_P = V_{BB}(1 - e^{-T/RC})$ or $\dfrac{V_P}{V_{BB}} = 1 - e^{-T/RC}$

or $\eta = 1 - e^{-T/RC}$ ($\because \eta = \dfrac{V_P - V_B}{V_{BB}}$ where (V_B is neglected)

or $e^{--\frac{T}{RC}} = 1 - \eta$

or $e^{\frac{T}{RC}} = \dfrac{1}{1-\eta}$

Taking logarithms on both sides, we have

$$\frac{T}{RC} = \log\left(\frac{1}{1-\eta}\right) \quad \text{or} \quad T = RC\log\left(\frac{1}{1-\eta}\right)$$

Therefore, the frequency of the saw tooth wave is given by

$$f = \frac{1}{T} = \frac{1}{CR\log[1/1-\eta]}$$

If we assume the capacitor discharge time to be zero, then T gives the time period of the voltage across 'C' which is a periodic saw tooth wave as sown in fig(2).

Short Questions and Solved Problems

1. What is meant by interbase resistance?

A. The total resistance between the two base terminals B_1 and B_2 of silicon bar is known as interbase resistance, when the emitter is open. It is represented by R_{BB} , i.e. $R_{BB} = R_{B1} + R_{B2}$

2. Why UJT is also called as double based- diode?

A As the two base terminals are taken from one section of the diode, the device is called double-based diode

3. What is an unijunction transistor?

A. A unijunction transistor is a three terminal silicon diode which has one emitter, and two base terminals. But it has only one junction. It has negative resistance.

4. What is the difference between UJT and conventional diode?

A. UJT is a three terminal silicon device and only one p-n junction and has three leads namely emitter and base 1 and base 2. But a junction diode has only two terminals namely p-type and n-type

5. What is meant by peak-point voltage?

A. The value of emitter voltage that causes the p-n junction to become forward biased is called peak-point voltage. This is expressed as $V_P = \eta V_{BB} + V_B$

6. What do you understand by intrinsic stand-off ratio?

A. The intrinsic stand -off ratio is the property of a UJT. The ratio R_{B1}/R_{BB} is called the intrinsic stand-off ratio, η.

Problems:

1. A given UJT has 20 volt between the bases. If the intrinsic stand off ratio is 0.6, find (i) stand off ratio (ii) peak-point voltage.

Solution: Given $V_{BB} = 20V$, $\eta = 0.6$ and for silicon $V_B = 0.7$

(i) Stand off voltage $= \eta V_{BB} = 0.6 \times 20 = 12$ V (ii) Peak-point voltage $V_P = \eta V_{BB} + V_B$

$= 12V + 0.7 = 12.7$ V.

2. A Silicon UJT has an inter base resistance of $10K\Omega$. Its intrinsic standoff ratio is 0.6. Find the values of resistances R_{B1} and R_{B2}.

Solution: Intrinsic stand off ratio $\eta = \frac{R_{B1}}{R_{BB}} \Rightarrow R_{B1} = \eta . R_{BB} = 0.6 \times 10K\ \Omega = 6K\Omega$

Therefore resistance $R_{B2} = 10K - 6K = 4K\ \Omega$

3. The interbase resistance of a silicon UJT is $10K\Omega$. It has $R_{B1} = 6K\Omega$ with $I_E = 0$. Find (i) UJT current if $V_{BB} = 20V$ and V_E is less than V_P (ii) Intrinsic standoff ratio (iii Peak point voltage.

Solution: Since $V_E < V_P$ and $I_E = 0$.

$I_{B1} = I_{B2} = \frac{V_{BB}}{R_{BB}} = \frac{20}{10K} = 20$mA, $\eta = \frac{R_{B1}}{R_{BB}} = \frac{6}{10} = 0.6$

$V_A = \eta V_{BB} = 0.6 \times 20 = 12V$, $V_P = \eta V_{BB} + V_B = 12 + 0.7 = 12.7V$.

UNIT – V: POWER SUPPLIES

Rectifiers:

Rectification: Rectification is the process by which an alternating supply voltage is converted into direct supply voltage. A rectifier is device which is used in rectification process.

P-N Junction Half Wave rectifier: Fig (1) shows the rectifying action of semiconductor diode. The A.C. voltage to be rectified is connected to the primary coil P of the power transformer. One end of the connected to N-region through a load resistor R.

Working of the rectifier:

During the first half cycle of A.C., one end of the secondary, say A becomes positive. Then the diode D is forward biased and hence current flows through the load R in the direction of arrows fig (1). During the next half cycle, the end A becomes negative and consequently, the diode D is reverse biased. Therefore, no current flows through the Load R. Thus we get a unidirectional current across R which flows in the form of half sine waves as shown in fig (1).

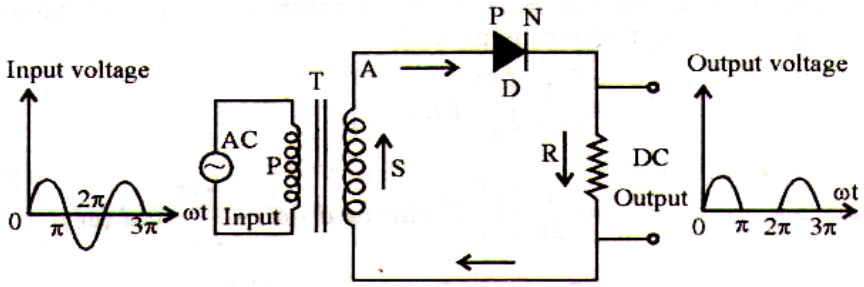


Fig (1)

Mathematical analysis:

Let the input voltage applied to the P-N junction diode in series with load R is given by

$$E = E_0 Sin\omega t$$

Then the instantaneous output current through the load resistance R is given by

$$I = \frac{E_0 Sin\omega t}{R_f + R} = I_0 Sin\omega t, \text{ When } 0 \le \omega t \le \pi$$

$$\text{And } I = 0, \qquad \text{When } \pi \le \omega t \le 2\pi$$

where R_f is the dynamic forward resistance of the semiconductor diode and $I_0 = = \frac{E_0}{R_f + R}$ is the peak value of the current.

D.C. (average) value of output current: The average d.c. current over one complete cycle is given by

$$I_{dc} = \frac{1}{2\pi}\int_0^{2\pi} id(\omega t) = \frac{1}{2\pi}\left[\int_0^{\pi} I_0 Sin\omega t.\, d(\omega t) + \int_{\pi}^{2\pi} 0.\, d(\omega t)\right]$$

$$= \frac{I_0}{2\pi}[-Cos\omega t]_0^{\pi} = \frac{I_0}{\pi}$$

$$\therefore I_{dc} = \frac{I_0}{\pi} = \frac{E_0}{\pi(R_f + R)} \qquad \rightarrow (1)$$

The d. c. (or average) output voltage across the load is given by

$$E_{dc} = I_{dc} \times R = \frac{I_0}{\pi} R = \frac{E_0}{(R_f + R)} \frac{R}{\pi}$$

(ii) R.M.S. (effective) value of output current: The root mean square value of the current, by definition, is given by

$$I_{rms} = \left[\frac{1}{2\pi}\int_0^{2\pi} I^2 d(\omega t)\right]^{\frac{1}{2}} = \left[\frac{1}{2\pi}\left\{\int_0^{\pi} {I_0}^2 Sin^2\omega t.\, d(\omega t) + \int_0^{2\pi} 0.\, d(\omega t)\right\}\right]^{\frac{1}{2}}$$

$$= \left[\frac{1}{2\pi}\int_0^{\pi} {I_0}^2 sin^2\omega t.\, d(\omega t)\right]^{\frac{1}{2}} = \frac{I_0}{2} \quad \rightarrow (2)$$

(iii) Power supplied to the circuit: The power supplied to the circuit from a.c. source is given by

$$P_{ac} = {I^2}_{rms}(R_f + \mathrm{R}) = \frac{{I_0}^2}{4}(R_f + \mathrm{R}) \quad \rightarrow (3)$$

(iv) Average power supplied to the Load R: The d.c. power output across the load R is given by

$$P_{dc} = {I^2}_{dc}\ \mathrm{R} = \frac{{I_0}^2 R}{\pi^2}$$

(v) Rectifier efficiency: The efficiency of the rectifier indicates how much a.c. power is converted into useful d.c. power. It is defined as the ratio of d.c. output power to the total a.c power supplied to the rectifier.

$$\text{i.e., } \eta = \frac{d.c.power\ supplied\ to\ the\ load}{Total\ a.c.input\ power} \times 100\%$$

$$\eta = \frac{P_{dc}}{P_{ac}} \times 100\% = \frac{{I_0}^2 R/\pi^2}{{I_0}^2(R+R_f)/4} \times 100\% = \frac{4R}{\pi^2}\frac{1}{(R_f+R)} \times 100\%$$

$$= \frac{400R}{\pi^2}\frac{1}{(1+R_f/R)}\% = \frac{40.6}{1+R_f/R}\%$$

If R_f << R, the efficiency is maximum. The theoretical maximum efficiency is obtained when $\frac{R_f}{R}$ = 0 and is equal to 40.6%.

Ripple factor: The output of the rectifier contains unidirectional (d.c.) current as well as a part of a.c. A measure of a.c. components is given by the ripple factor 'γ' which is defined as

$$\gamma = \frac{r.m.s.\ value\ of\ a.c.components\ of\ the\ output}{average\ or\ d.c.component\ of\ the\ output}$$

$$= \frac{I'_{rms}}{I_{dc}} = \sqrt{\left\{\frac{I^2 rms}{I^2 dc} - 1\right\}}$$

But for half wave rectifier, using equations (1) and (2), $\frac{I_{rms}}{I_{dc}} = \frac{I_0/2}{I_{0/\pi}} = \frac{\pi}{2}$

$$\therefore \gamma = \sqrt{\left[\left(\frac{\pi^2}{4}\right) - 1\right]} = 1.21$$

Thus for a half wave rectifier $\gamma > 1$ or $I'_{rms} > I_{dc}$

i.e., the a.c. component of the output exceeds the d.c.value. It indicates that half wave rectifier is a poor device for converting a.c. into d.c.

Peak inverse voltage: Peak inverse voltage is defined as the maximum reverse voltage across the diode when diode is in non conducting mode. i.e., PIV = E_0

Voltage regulation: Voltage regulation is the ability of a rectifier to maintain a specified output voltage irrespective of the variation in the load resistance

For half wave rectifier $I_{dc} = \frac{I_0}{\pi} = \frac{E_0}{\pi(R_f+R)}$

Or $I_{dc}(R_f + R) = \frac{E_0}{\pi}$

Or $I_{dc}\mathrm{R} = \frac{E_0}{\pi} - I_{dc}R_f$

Or $E_{dc} = \frac{E_0}{\pi} = \frac{E_0}{\pi} - I_{dc}R_f$

When I_{dc}= 0, E_{dc} has its maximum value $\frac{E_0}{\pi}$. As I_{dc} increases, E_{dc} decreases linearly depending on the value of R_f. Therefore, voltage regulation of half wave rectifier is poor.

Full Wave Rectifier using Centre tapped Transformer:

Fig (1) shows the circuit of centre tap full wave rectifier employing two P-N junctions D_1 and D_2. The P-regions of the diodes are connected to the ends A and B of the secondary of the transformer; the middle point C is connected to the junction of N-regions through the load resistance 'R '.

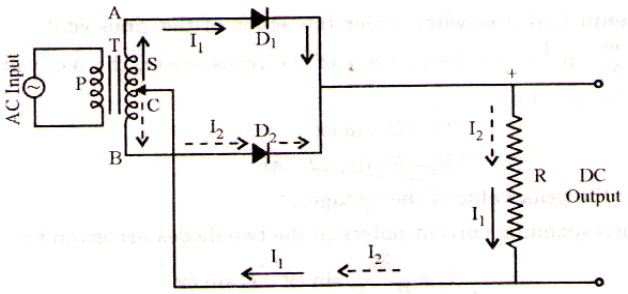


Fig (1)

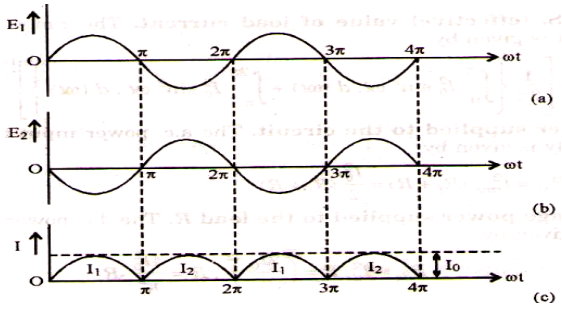


Fig (1) (a,b,c) input & output Waveforms

Working of the rectifier:

During the positive half cycle of secondary voltage, one end of the secondary say, A becomes positive and end B becomes negative. Consequently, the diode D_1 is forward biased and a current I_1 flows in the circuit in the direction AD_1RCA show by solid arrows. During this time the diode D_2 is reverse biased and hence no current flows through it. During the negative half cycle of AC input, end A becomes negative and end B positive. Consequently diode D_2 is forward biased and a current I_2 flows in the circuit through D_2 along BD_2RCB as shown by the dotted arrows. During this period D_1 is reverse biased and hence does not conduct.

Thus the diodes D_1 and D_2 conduct alternately and each time the current through the load R flows in the same direction. Consequently, the resulting output current is unidirectional and flows in the form of half sine waves as shown in fig 1(c).

Mathematical analysis: when a sinusoidal voltage of frequency is applied to the primary of the transformer, the a.c. voltage across AC and BC are given by

$E_1 = E_0 \text{Sin}\omega t$

$E_2 = E_0 \text{ Sin } (\omega t - \pi)$ Where E_0 is the peak value of the voltage

The corresponding current pulses in the two diodes are given by

$$I_1 = \frac{E_0}{(R_f+R)} \text{Sin}\omega t = I_0 \text{Sin}\omega t, \text{ and } I_2 = 0, \text{ when } 0 < \omega t < \pi$$

And $I_1 = 0$, and $I_2 = \frac{E_0}{(R_f+R)} \text{Sin}\omega t = -I_0 \text{Sin}\omega t$, $\pi < \omega t < 2\pi$

Where R_f is the dynamic forward resistance of semiconductor diode.

(i)D.C. (average) value of output current: Since the currents I_1 and I_2 are of the same form (I =$I_0 Sin\omega t$), the average or d.c. value of current is given by

$$I_{dc} = \frac{1}{\pi}\int_0^{\pi} Id(\omega t) = \frac{1}{\pi}\int_0^{\pi} I_0 Sin\omega t d(\omega t)$$

$$I_{dc} = \frac{2I_0}{\pi} \longrightarrow (1)$$

The d.c. output voltage across the load R is therefore,

$$E_{dc} = I_{dc} \times R = \frac{2I_0 R}{\pi} = \frac{2R}{\pi}\frac{E_0}{(R_f+R)} \longrightarrow (2)$$

(ii) R.M.S (effective) value of the load current: The r.m.s. value of the total output current is given by

$$I_{rms} = \left[\frac{1}{2\pi}\left\{\int_0^{\pi} {I_0}^2 Sin^2\omega t d(\omega t) + \int_{\pi}^{2\pi} {I_0}^2 Sin^2\omega t d(\omega t)\right\}\right]^{\frac{1}{2}} = \frac{I_0}{\sqrt{2}} \longrightarrow (3)$$

(iii) Power supplied to the circuit: The a.c. power input to the rectifier from the supply is given by

$$P_{ac} = I^2{}_{rms}(R_f + \mathrm{R}) = \frac{{I_0}^2}{2}(R_f + \mathrm{R}) \qquad \rightarrow (4)$$

(iv) Average power supplied to the load resistance R: The d.c. power supplied to the load R is given by

$$P_{dc} = I^2{}_{dc}\ \mathrm{R} = \left(\frac{2I_0}{\pi}\right)^2 R = \frac{4{I_0}^2 R}{\pi^2}\mathrm{R} \qquad \rightarrow (5)$$

(v) Rectifier efficiency: The efficiency of a rectifier is defined as the ratio of the d.c. output power to the a.c. power supplied to the circuit. It is denoted by the symbol 'η '.

$$\text{i.e., } \eta = \frac{d.c.power\ supplied\ to\ the\ load}{Total\ a.c.input\ power} \times 100\%$$

$$\eta = \frac{P_{dc}}{P_{ac}} \times 100\% = \frac{4{I_0}^2 R/\pi^2}{{I_0}^2(R+R_f)/2} \times 100\% = \frac{8}{\pi^2}\frac{1}{(1+R_f/R)} \times 100\% = \frac{81.2}{1+R_f/R}\%$$

If R_f << R, the efficiency is maximum. The theoretical maximum efficiency is obtained when $\frac{R_f}{R} = 0$ and is equal to 81.2% only.

(vi) Ripple factor: The output of a rectifier contains unidirectional (d.c.) current as well as a part of a.c. A measure of a.c. components is given by the ripple factor 'γ' and is defined as

$$\gamma = \frac{r.m.s.\ value\ of\ a.c.components\ of\ the\ output}{average\ or\ d.c.component\ of\ the\ output}$$

$$= \frac{I'_{rms}}{I_{dc}} = \sqrt{\left\{\frac{I^2 rms}{I^2 dc} - 1\right\}}$$

Using equations (1) & (3) $\gamma = \frac{I_{rms}}{I_{dc}} = \frac{I_0/\sqrt{2}}{2I_{0/\pi}} = \frac{\pi}{2\sqrt{2}}$

$$\therefore \text{ Ripple factor, } \gamma = \sqrt{\left[\left(\frac{\pi^2}{8}\right) - 1\right]} = 0.48$$

Thus the d.c. output voltage of the full wave rectifier has a small ripple.

(vii) Peak inverse voltage: Peak inverse voltage is defined as the maximum reverse voltage across the diode when it is reverse biased. (or non conducting).

i.e., PIV = $2E_0$ (peak voltage)

(viii) Voltage regulation: Voltage regulation is the ability of a rectifier to maintain a specified output voltage irrespective of the variation in the load resistance.

For full wave rectifier, $I_{dc} = \frac{2I_0}{\pi} = \frac{2E_0}{\pi(R_f+R)}$

$$\text{or } I_{dc}(R_f + R) = \frac{2E_0}{\pi}$$

$$\text{or } I_{dc}\mathrm{R} = \frac{2E_0}{\pi} - I_{dc}R_f$$

$$\text{or } E_{dc} = \frac{2E_0}{\pi} - I_{dc}R_f$$

Thus full wave rectifier provides larger d.c. output voltage and good regulation in comparison with half wave rectifier. It can supply larger load current as compared to half wave rectifier.

Full Bridge rectifier or (double way rectifier):

Fig (1) shows the circuit of a full wave bridge rectifier using four P-N junction diodes D_1, D_2, D_3, D_4.

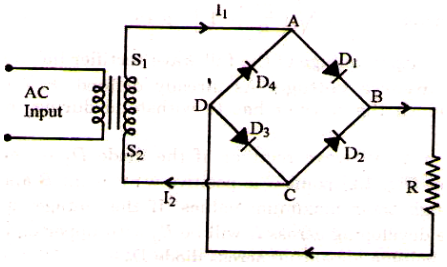


Fig.(1)

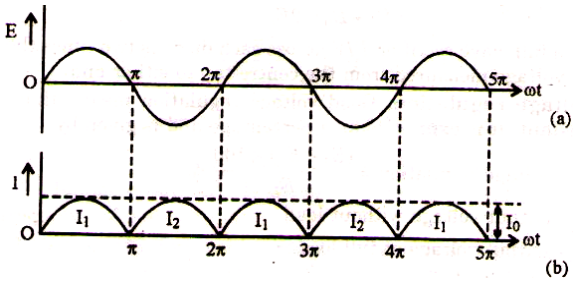


Fig.(1b)

Working of Bridge Rectifier: During the +Ve input half cycle, terminal M of the secondary of the transformer is +Ve while the terminal N is –Ve. In this situation diodes D_1 and D_3 are forward biased (ON) i.e they conduct whereas diodes D_2 *and* D_4 are reverse biased (OFF) i.e they do not conduct. So a current flows along ABDCS$_2$S$_1$ as shown by arrow in the fig (1). There will be a voltage drop acrossR_L.

During the –Ve input half cycle, terminal N of the secondary of transformer becomes +Ve while the terminal M becomes –Ve. Under this situation diodes D_2 *and* D_4 are forward biased (ON) i.e they conduct whereas D_1 and D_3 are reverse biased (OFF) i.e they do not conduct. Now a current flows along CBDAS$_1$S$_2$ as shown by dotted arrow in fig (1). The current produces a voltage drop acrossR_L. It is obvious from figure that the current through load resistanceR_L is in the same direction BC during the both half cycles of the input a.c. supply. The output waveforms are shown in fig (1b). Here the wave form of the load current is essentially the same as in case of full wave rectifier. It is evident that two diodes conduct simultaneously in series. Therefore, the current pulses are represented by

$$I_1 = \frac{E_0}{(2R_f+R)} \text{Sin}\omega t = I_0 \text{Sin}\omega t, \text{ and } I_2 = 0, \text{ when } 0 < \omega t < \pi$$

and $$I_1 = 0, \text{ and } I_2 = \frac{E_0}{(2R_f+R)} \text{Sin}\omega t = I_0 \text{Sin}\omega t\ , \pi < \omega t < 2\pi$$

Where R_f is the dynamic forward resistance of each diode and I_0 is the maximum current given by,

$$I_0 = \frac{E_0}{(2R_f+R)}$$

The expression for average d.c. current $\left(= \frac{2I_0}{\pi}\right)$r.m.s. value of current $\left(= \frac{I_0}{\sqrt{2}}\right)$ and ripple factor (= 0.48) are the same as in case of centre tap full wave rectifier but the rectifier efficiency is given by

$$\eta = = \frac{81.2}{1+2R_f/R}\%$$

PRV (Peak Reverse Voltage):

It is defined as the voltage across each diode when the diode is reverse biased (or the diode is in non conducting mode) and is equal to E_0, i.e. the voltage across the secondary of the transformer.

i.e., PIR = E_0 (Peak value)

Comparison between Half wave and full wave rectifiers:

Term	Half Wave	Full Wave
1.Average/d.c. current	I_m/π	$2I_m/\pi$
2.d.c. voltage	$V_m/\ \pi$	$2V_m/\ \pi$
3.RMS current	$I_m/2$	$I_m/\sqrt{2}$
4.Efficiency	40.6%	81.2%
5.Ripple factor	1.21	0.48
6.PIV	V_m	$2V_m$

Filters: We know that the output of a rectifier consists a d.c. component as well as a.c. component, known as ripple. In most of the electronics circuits or devices, a pure d.c. is required. This is achieved with the help of a circuit known as a filter circuit or smoothing circuit. The filters minimize ripples either by passing or preventing the a.c. components and provide a regulated constant voltage.

Shunt Capacitor filter:

The simplest type of smoothing circuit is a shunt capacitor filter obtained by placing a capacitor C in parallel with the load resistance R as shown in Fig (1). It is an effecting way of filtering the a.c. components from the output of the rectifier. The capacitor is chosen that its reactacne

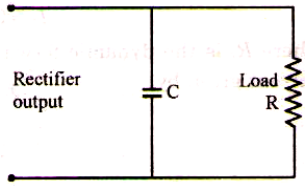


Fig.(1)

is so chosen that its reactance $\left(\frac{1}{\omega C}\right)$ at the frequency of a.c mains is very small as compared to the load R. Then the a.c. components or ripple flowing through the load are mostly bypassed. Thus the ripple flowing through the load decreased or filtered from the output.

The ripple factor of the filter is given by $\gamma = \frac{1}{4\sqrt{3}fCR}$

Thus, the ripple factor varies inversely with the time constant CR of the filter and also inversely with the load resistance R. It is less for larger R. For R = α, the ripple is zero.

This expression shows that ripple factor decreases if R decreases or Load current increases. The filtering is poorest at no load (R = α, open circuit) for which the above equation becomes $\gamma = \frac{\sqrt{2}}{3} = 0.47$ .which almost the result when no filter is used.

The L-section filter or inductor filter:

We have seen that series inductor filter an shunt capacitor filter are not much efficient to provide low ripple at all loads.

The capacitor filter has low ripple at heavy loads while inductor filters at small loads. A combination of these two filters may be selected to make the ripple independent of load resistance. The resulting filter is called L-type choke input filter shown in fig (1).

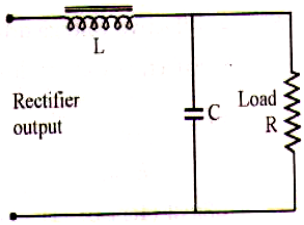


Fig (1)

In this type of filter the series inductor L readily passes the d.c. components that remain after passing through L are bypassed by the shunt capacitor C which offers a low reactance $\left(\frac{1}{\omega C}\right)$ to them but an infinite resistance to d.c. Thus output across the load possesses less a.c. components or the lower ripple factor.

The ripple factor of the L-section filter is given by

$\gamma = \frac{0.47}{4\omega^2 L^2 - 1}$. Thus the ripple factor does not depend upon the load resistance R.

The π – section filter or capacitor input filter:

When higher output voltage at light loads is desired, an input capacitor is added to L-section filter to form a π- section filter.

This π– section filter provides an output voltage that approaches the peak value of the a.c. of the source, the ripple components being very small. Such a filter is illustrated in fig (1).

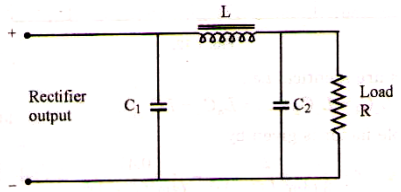


Fig. (1)

The π-type filter may be considered to be made up of the following two components:

(i)Capacitor filter formed by capacitor C_1

(ii) Inductor input filter formed by choke L and capacitorC_2.

The capacitor C_1 is periodically charged to almost the peak value of the rectifier output. Between successive charging process, the voltage across the capacitor falls exponentially due to its discharge through the L-section filter and the load, but remains very near to the peak value. The remaining pulsations in the current are opposed by the series choke L and bypassed to ground by capacitor C_2 . Thus the π-section filter produces a unidirectional output voltage across load R with negligible ripple.

The ripple factor of the π – section filter is given by

$$\gamma_\pi = \frac{5.7\times 10^3}{C_1 C_2 LR} \quad \rightarrow (1)$$

From equation (1) we may seen that the ripple factor γ_π of the capacitor input π-section filter varies inversely with the load resistance R or increase with the load current.

Regulated Power Supplies

Electronic circuits (using diodes, transistors etc) require a source of D C Power supply. Regulated D C power supply is one which keeps the D C voltage at a specified value irrespective of the variations in input voltage and load current.

Voltage regulation: Voltage regulation is defined as the ability of voltage regulator to maintain a specified output voltage irrespective of the variations in the load resistance and the variations in the input voltage. It is expressed in percentage and is given by

$$\text{Voltage regulation} = \frac{(V_{NL} - V_{FL}) \times 100}{V_{FL}} \ \%$$

where V_{NL} = output voltage without load

and V_{FL} = output voltage at full load.

Types of voltage regulators:

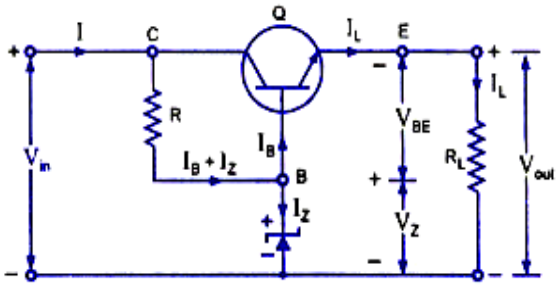
They are two basic types of voltage regulators. They are 1. Transistor series voltage regulator

2. Transistor shunt voltage regulator

Transistor series voltage regulator:

The circuit of a transistor series voltage regulator is shown in Fig(1). Here transistor behaves like a variable resistor which is determined by the base current.

Applying the Kirchhoff's law, the output voltage V_0 across the load resistor R_L given by



Transistor Series Voltage Regulator

Fig (1)

$$V_Z - V_{BE} - V_0 = 0$$

$$V_0 = V_Z - V_{BE}$$

and $V_{BE} = V_Z - V_o \quad \rightarrow (1)$

Working: Now suppose R_L is decreased to get more current.Then V_0 will tend to decrease. Since zener voltage V_Z is fixed, it will increase V_{BE} (refer eqn. 1). Consequently, forward bias of the transistor will increase; thereby increasing its level of conduction. This decreases the voltage drop between C & E of the transistor. As a result, collector- emitter resistance of the transistor will decrease. It will slightly increase the current to compensate for decrease in R_L and increase output voltage. Consequently, the output voltage $V_o = I_L R_L$ will remain at constant value and we get a regulated voltage across the load resistor R_L. The circuit action may be summarized in the following equation.

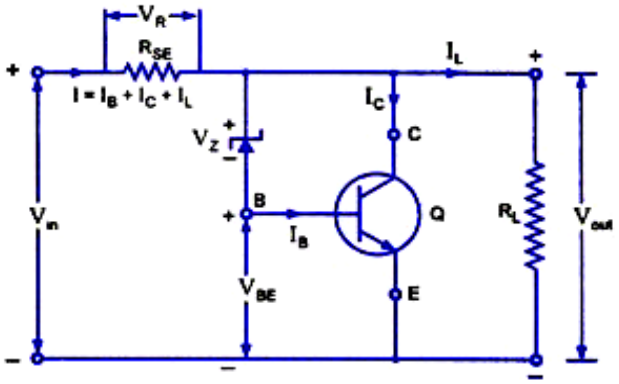
$$V_0 \downarrow \rightarrow VBE \uparrow \rightarrow V_{CE} \downarrow \rightarrow V0 \uparrow.$$

Transistor shunt voltage regulator:

The circuit of a transistor shunt voltage regulator is shown in Fig. (2). Here the transistor is connected in shunt. Since path AB is in parallel to the output voltage V_o across the load resistor R_L, we have from Kirchhoff's voltage law

$$V_0 - V_Z - V_{BE} = 0$$

$$\text{or} \quad V_{BE} = V_0 - V_Z \qquad \rightarrow (1)$$



Transistor Shunt Voltage Regulator

Fig.(2).

Working: Since, zener voltage V_Z is fixed, any increase or decrease in V_0 will have a corresponding effect on V_{BE}. Suppose V_0 decreases, then from equation (1), V_{BE} will also decrease (since V_Z is fixed). Consequently, I_B decreases.

Therefore, I_C ($= \beta I_B$) will also decrease. It will lead to a decrease in I ($= I_B + I_C + I_L$). Consequently, voltage ($V_R = IR$) across the resistor R will decrease. As a result, output voltage V_O will increase because

$$V_{in} = V_R + V_O$$

$$\text{or} \quad V_O = V_{in} - V_R$$

Thus the output voltage will remain at constant value or we get regulated voltage across R_L.

The circuit action may be summarized in the following eqn.

$$V_0 \downarrow \rightarrow V_{BE} \downarrow \rightarrow I_B \downarrow \rightarrow I_C \downarrow \rightarrow I \downarrow \rightarrow V_R \downarrow \rightarrow V_0 \uparrow$$

Block diagram of regulated DC power supply and function of each block:

[Q. Draw the block diagram of regulated DC power supply and explain the function of each block]

All electronic equipments contain a circuit that converts ac supply into dc supply called DC regulated power supply whose output is a constant dc voltage connected to all parts of the equipment for operation. In general at the input of the power supply there is a power transformer. It is followed by a rectifier (a diode circuit), a smoothing filter and then by a voltage regulator circuit as shown in Fig.(1)

Fig (1) shows the block diagram of a regulated DC power supply. Let us explain function of each block of the DC power supply.

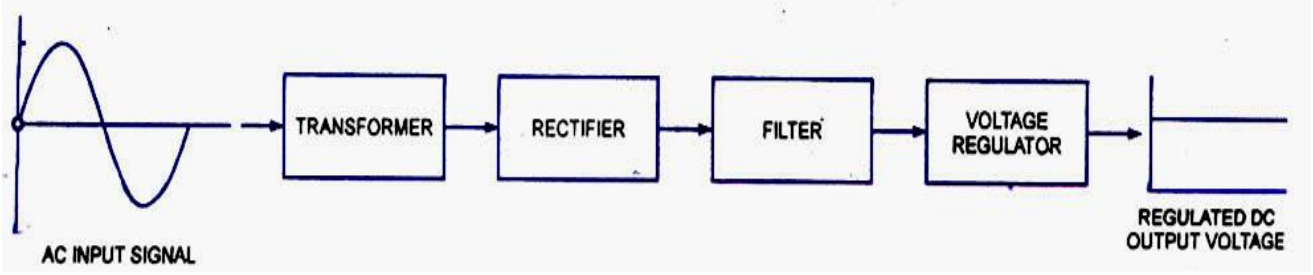


Fig.1. Block diagram of regulated D C power supply

Transformer is used to step-up or step-down (usually to step-down) the-supply voltage as per need of the electronic devices and circuits. A C voltage from mains (220V/50Hz) is transformed into desired A C voltage by the power transformer.

Rectifier is a device which converts the ac voltage into pulsating dc. Here, the AC voltage from transformer is converted into pulsating DC by the rectifier. The rectifier typically needs one, two or four diodes. Rectifiers may be either half-wave rectifiers or full-wave rectifiers **(**centre-tap **or** bridge**)** type.

The output voltage from a rectifier circuit has a pulsating character i.e., it contains unwanted ac components along with dc component. To reduce ac components from the rectifier output voltage a filter circuit is required.

Filter is a device which passes dc component to the load and blocks (stops) ac components of the rectifier output. Filter is constructed using capacitors and/or inductors and resistors.

The magnitude of output dc voltage may vary with the variation of either the input ac voltage or the magnitude of load current. So at the output of a filter a voltage regulator is required, to provide an almost constant dc voltage at the output of the regulator.

The **voltage regulator** may be constructed using a Zener diode, and or electronic devices such as transistors, ICs etc. Its main function is to maintain a constant dc output voltage.

Three terminal Voltage Regulators (IC 78XX and 79XX):

[Q: Explain in detail about 3 terminal IC voltage regulators.]

Three terminal Voltage Regulator IC **usually** have three leads. It converts varying DC input voltage into a constant regulated output voltage. They are available in a variety of outputs.

The most common numbers are 78 or 79 and finish with two digits indicating the output voltage. The number 78 represents positive voltage and 79 negative one. The 78XX series of voltage regulators are designed for positive input. And the 79XX series is designed for negative input.

Examples:

1. 5V DC Regulator Name: LM7805
2. -5V DC Regulator Name: LM7905
3. 15V DC Regulator Name: LM7815
4. -9V DC Regulator Name: LM7909

Three terminal IC Voltage Regulators are used due to the following reasons:

1. Easy to fabricate and lower cost
2. Fairly simple and fixed voltage types of high quality precision regulators.
3. Having unique built in features such as current limiting, self protection against temperature etc.

The three terminal IC is shown in fig. (1a). The three terminals of IC voltage regulator are labeled as (1) Input (2) Ground and (3) Output. It produces a constant regulated output voltage from varying DC voltage.

Fig.1(a)

Fig. 1(b)

The circuit diagram of a typical IC voltage regulator is shown in Fig. (2a). Here unregulated dc voltage is connected to input leg (which can hold up to 36V DC), Common leg (GND) is grounded and

regulated DC output voltage is taken from output leg. The capacitor C_1, parallel between input leg and the common is used to reduce ripple voltage, if any. For maximum voltage regulation, a capacitor C_2 is connected in parallel between the output and common leg. It also eliminates any high frequency AC voltage that could otherwise combine with the output voltage.

Fig.2(a)

Fig. (2b) shows the circuit diagram of adjustable voltage regulator using 78XX IC voltage regulator.

The output voltage is given by equation

$$V_{OUT} = V_{FIXED} + \left[\frac{V_{FIXED}}{R_1} + I_Q \right] R_2$$

For example, for a 7805 IC regulator, V_{FIXED} = 5V. Let $R_1 = R_2$ = 1K Ω and I_Q = 5 mA, then its output voltage is

Fig.(2b)

$$V_{OUT} = 5 + \left[\frac{5V}{1K} + 5mA \right] x1K\ \Omega$$

$$= 5 + [5mA + 5mA]\ x1K\ \Omega = 5 + (10mA\ x1K\ \Omega) = 5 + 5 = 15\ V$$

Thus output of IC 7805 is adjusted anywhere between 5V to 15 V using external resistances R_1 and R_2.

***Note:** As a general rule the input voltage should be limited to 2 to 3 volts above the output voltage. If the input voltage is unnecessarily high, the regulator will overheat. Unless sufficient heat dissipation is provided through heat sinking, the regulator will shut down.

Switch-Mode Power Supply (SMPS) :

A switch mode power supply circuit can be used to step up or step down an unregulated dc input voltage to produce a regulated dc output voltage.

The advantages of SMPSs are compact in size, light weight and highly efficient. More over, SMPSs are reliable, efficient and cool running. They are commonly found in battery operated equipment like laptops computers and CD players.

Switched power supplies are more efficient and they tend to have an efficiency of 80% or more. They can be packaged in a fraction of the size of linear regulators. Unlike linear or ordinary regulators, switch mode power supplies can step up or step down the input voltage.

Principle of operation:

In a switched-mode power supply (SMPS), the AC mains input is directly rectified and then filtered to obtain a DC voltage. The resulting DC voltage is then switched on and off at a high frequency by electronic switching circuitry, thus producing an AC current that will pass through primary of a high-frequency transformer. Switching occurs at a very high frequency (typically 10 kHz — 1 MHz), thereby enabling the use of transformers and filter capacitors that are much smaller, lighter, and less expensive than those found in linear power supplies operating at mains frequency. After the transformer secondary, the high frequency AC is rectified and filtered to produce the DC output voltage.

Block diagram of SMPS with output voltage regulation and theory of operation:

Q: Draw the Block diagram of SMPS with output voltage regulation and explain its theory of operation.

Block diagram of a mains operated AC/DC SMPS with output voltage regulation is shown in Fig.(1). Let us explain function of each block of the SMPS power supply.

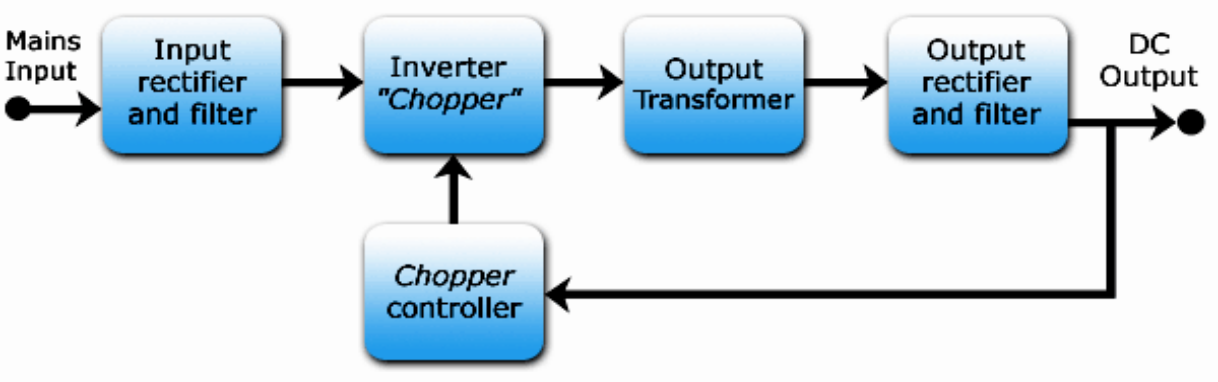


Fig.(1). Block diagram of SMPS with output voltage regulation

Input rectifier stage

The first stage of SMPS is a full-wave rectifier to convert AC mains input to DC voltage. This is called rectification. The rectifier produces an unregulated DC voltage which is then sent to a large filter capacitor.

Inverter stage

The inverter stage converts DC to AC by running it through a power oscillator, whose output transformer is very small with few windings at a frequency of tens or hundreds of kilohertz. The switching is implemented as a multistage (to achieve high gain) MOSFET amplifier.

Voltage converter and output rectifier

If the output is required to be isolated from the input, as is usually the case in mains power supplies, the inverted AC is used to drive the primary winding of a high-frequency transformer. This converts the voltage up or down to the required output level on its secondary winding. The output transformer in the block diagram serves this purpose.

If a DC output is required, the AC output from the transformer is rectified. For output voltages above ten volts or so, ordinary silicon diodes are commonly used. For lower output voltages, MOSFETs may be used.

The rectified output is then smoothed by a filter consisting of inductors and capacitors. For higher switching frequencies, components with lower capacitance and inductance are needed.

Regulation

A feedback circuit monitors the output voltage and compares it with a reference voltage, which shown in the block diagram serves this purpose.

Applications:

1. A switch mode power supply is found in battery operated equipment like laptops computers, CD players, Television receiver, Battery charger etc.
2. A switch mode power supply circuit can be used to step up or step down an unregulated dc input voltage to produce a regulated dc output voltage.

Advantages:

The advantages of SMPSs are compact in size, light weight and and highly efficient. More over, SMPSs are reliable, efficient and cool running.